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Synthesis, Characterization and Applications of Barium Strontium Titanate Thin Film Structures

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Synthesis, Characterization and Applications of Barium Strontium
Titanate Thin Film Structures

by

Supriya Ketkar

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
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Keywords: RF magnetron sputtering, Corona-Kelvin metrology,
supercapacitors, sol-gel deposition, frequency tunable

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Dedication

I dedicate this work to my parents, Mr. Ashok Balwant Ketkar and Mrs. Anuprita Ashok Ketkar, for always being there for me in every way possible. Without their unflinching support and patience, I would not have been able to finish my task at hand.

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Abstract

Barium Strontium Titanate (BST) based ferroelectric thin film devices have been popular over the last decade due to their versatile applications in tunable microwave devices such as delay lines, resonators, phase shifters, and varactors. BST thin films are promising candidates due to their high dielectric constant, tunability and low dielectric loss. Dielectric-tunable properties of BST films deposited by different deposition techniques have been reported which study the effects of factors, such as oxygen vacancies, film thickness, grain size, Ba/Sr ratio, etc. Researchers have also studied doping concentrations, high temperature annealing and multilayer structures to attain higher tunability and lower loss. The aim of this investigation was to study material properties of Barium Strontium Titanate from a comprehensive point of view to establish relations between various growth techniques and the film physical and electrical properties.

The primary goal of this investigation was to synthesize and characterize RF magnetron sputtered Barium Strontium Titanate ($Ba_{1-x}Sr_xTiO_3$), thin film structures and compare their properties with BST thin films deposited by sol-gel method with the aim of determining relationships between the oxide deposition parameters, the film structure, and the electric

field dependence. In order to achieve higher thickness and ease of fabrication, and faster turn around time, a 'stacked' deposition process was adopted, wherein a thin film (around 200nm) of BST was first deposited by RF magnetron sputtering process followed by a sol-gel deposition process to achieve higher thickness. The investigation intends to bridge the knowledge gap associated with the dependence of thickness variation with respect to the tunability of the films. The film structures obtained using the three different deposition methods were also compared with respect to their analytical and electrical properties. The interfacial effect on these 'stacked' films that enhance the properties, before and after annealing these structures was also studied.

There has been significant attention given to Graphene-based supercapacitors in the last few years. Even though, supercapacitors are known to have excellent energy storage capability, they suffer from limitations pertaining to both cost and performance. Carbon (CNTs), graphene (G) and carbon-based nanocomposites, conducting polymers (polyaniline (PANI), polypyrrole (PPy), etc.) have been the fore-runners for the manufacture of supercapacitor electrodes. In an attempt to better understand the leakage behavior of Graphene Polyaniline (GPANI) electrodes, BST and BST thin films were incorporated as constituents in the process of making supercapacitor electrodes resulting in improved leakage

behavior of the electrochemical cells. A detailed physical, chemical and electrochemical study of these electrochemical cells was performed.

The BST thin films deposited were structurally characterized using Veeco Dektak thickness profilometer, X-ray diffraction (XRD), Scanning electron microscopy (SEM) and atomic force microscopy (AFM) techniques. The interfacial structural characterization was carried out using high-resolution transmission electron microscopy (HRTEM). This investigation, also presents noncontact electrical characterization of BST films using Corona Kelvin metrology (C-KM).

The 'stacked' BST thin films and devices, which were electrically tested using Corona Kelvin metrology, showed marked improvement in their leakage characteristics over both, the sputtered and the sol-gel deposited counterparts. The 'stacked' BST thin film samples were able to withstand voltages up to 30V positive and negative whereas, the sol-gel and sputtered samples could hold only up to a few volts without charge leaking to reduce the overall potential. High frequency, 1GHz, studies carried out on BST thin film interdigitated capacitors yielded tunability near 43%.

Leakage barrier studies demonstrated improvement in the charging discharging response of the GPANI electrochemical electrodes by 40% due to the addition of BST layer.

Chapter 1: Introduction and Organization of Dissertation

Motivation

The electronics market is driven by device speed, functionality and cost. Moore's law has been the governing factor in controlling the device dimensions and propelling the industry in miniaturizing the chips and digging deep into newer materials and processes. Similarly, there is a huge demand on reducing the speed of operations and increasing the bandwidth of possible communication channels. Currently, transistor dimensions in mass manufacture have shrunk to 14nm [1]. To 'keep up' with Moore's Law, industrial research has been exploring nanotechnology, low-k dielectric materials and novel-transistor structures [2-4]. Application areas include logic, memory, energy storage and nanotube transistors for RF purposes [5-8]. Smarter communication devices demand higher frequency allocations pushing RF engineers to look into THz (terahertz) range for amplifier, transmitters/receivers and antennas. Thus, there is an increased demand for communications to multiple systems, all communicating at different frequencies, with the same structure. Materials and devices with such ability are referred to as frequency agile.

At the same time, there have to be novel materials introduced to improve already existing power requirements [5, 9]. Portable computing and smart communication devices present the need for higher, and longer delivery, power sources. This may be addressed by curbing battery power leakage issues, improving the battery life.

Problem Definition

Increased demand for frequency agile wireless communication devices directly relates to tunable front end RF components. Barium Strontium Titanate (BST), thin films have been widely researched for their highly tunable, frequency agile property by scientists all over the world for the past decade [6, 10-13]. BST thin films have been promising candidates due to their high dielectric constant, tunability and low dielectric loss. Dielectric-tunable properties of BST films deposited by different deposition techniques have been reported which study the effects of different deposition factors, film thickness, etc. Even though much literature is available, there are some aspects, which have not been fully developed. A thorough understanding of different processes of deposition that work together to form epitaxial films of BST and their leakage behavior was missing.

Use of BST as a leakage barrier in supercapacitor applications is a novel approach and was investigated in detail. Currently, no reports have been produced to our knowledge on this topic. Achieving improved properties in this arena should enhance the understanding of BST structures

and demonstrate a comprehensive approach to achieve better and faster electronic devices, as well as longer battery life of energy storage products.

State-of-the-art BST Technology

The processing and characterization of typical semiconductor devices, made from silicon, gallium arsenide, or germanium is well understood and their processing technologically is mature [14]. The change in tunability of semiconductor varactor diodes is achieved by the variation of the depletion region width, which in turn, is achieved by changing the reverse biased electrical field applied to the junction. This change in capacitance can be achieved by changing the width of the channel in the semiconductor varactor or changing the thickness of the dielectric material in a parallel plate capacitor. Varying the doping in the layers can also change the tunability. But lightly doped layers can be resistive causing the varactor diode to be lossy at RF and microwave frequencies [15]. Because of the way semiconductor device switching works, they suffer from poor power handling capability along with increased losses at high frequencies [16].

Another technology that can be used for making tunable devices is that of RF MEMS. RF MEMS are physical switches and have moving parts [17]. RF switches have high isolation but because of the mechanical movement, there are drawbacks due to mechanical wear and tear and friction. They also suffer from cohesive force issues. They suffer from slower

switching speeds ($>1s$) due to the moving cantilevers [18]. Additionally, RF MEMS also suffer from low tunability and noise effects [14, 18].

The past few decades have seen an improvement in tunable RF devices and microwave components due to the advent of ferroelectric materials [19-22]. Ferroelectric material permittivity changes may be induced by variation in the applied electric field. Usually, when the material is used as a dielectric in capacitors, it behaves like a varactor, due to the capacitance changing property of the material with the applied potential. Ferroelectric varactors have comparable tunabilities relative to semiconductor varactors [23] along with better switching speeds and low losses [24]. At the same time, varactors made from ferroelectric materials will be less prone to fail mechanically as compared to MEMS switches. The only drawback with using ferroelectric devices is that they must be operated above the Curie temperature to avoid the hysteresis.

Research Objectives

The main objectives of this research are summarized below:

- Deposit BST thin films using different deposition methods (sputtering, sol-gel and stacks of these two) and compare the physical and electrical properties of these films. This will lead to a better understanding of which process to select for depositing the thin films

depending on the advantages and disadvantages of the process parameters of the end product.

- Relate the physical attributes of BST thin films to their electrical properties, and get a better understanding of the electrical phenomenon that take place.
- Study the electrical properties of these BST thin films using non-contact Corona Kelvin Metrology (C-KM). This method permits dielectric characterization of as-produced films derived from sequences of charge deposition and associated non-contact potential determination.
- Vary the thickness of BST thin films and study the variation in their tunability. Using three different approaches, it was possible to achieve the desired thickness of BST thin films. A thorough physical and electrical characterization has been undertaken to understand the effect of thickness variation.
- Understand the effect of using a thin film of BST as a 'protective' layer on Graphene Polyaniline (G-PANI) electrochemical cell electrodes for supercapacitor applications. This study was necessary to understand the mechanism of BST playing the role of a leakage minimizing barrier layer.

Research Contributions

The most important contributions of this dissertation are advancing the understanding of the dielectric electrical leakage behavior of layers of BST thin film deposited using rf magnetron sputtering, sol-gel and a combination of the methods. Various parameters were considered while investigating the electrical properties of these thin films. Parameters include, thin film quality, film thickness and film structure. The annealing temperature and annealing gas chemistry were other factors, which affected the films and their electrical properties. It was found that, a combination of the sputtering and sol-gel deposition processes was a faster approach to get thicker and more reliable thin films. Combining the two deposition methods, lead to a reduction in thermal budget due to the samples being exposed to elevated temperatures for a shorter duration. The 'stack' layer has misaligned crystal orientation at the sputtered/sol-gel thin film interface which leads to better charge retention in the films.

Inter-digited capacitor patterns with different geometries were fabricated on Alumina substrates and electrically tested at 1 GHz frequency over an electric potential range of 0V to 90 V. This study was carried out to estimate the tunability of the films. It was found that the tunability of the films was near 43% at 50 V. This tunability is well suited for applications in high frequency communication devices, where high tunability with low dielectric loss is desirable.

Another aspect of this investigation involved understanding the leakage behavior of Graphene-polyaniline (GPANI) electrochemical cells for supercapacitor applications. The approach utilized a thin layer BST film on GPANI, which improved the electrochemical properties of the structure. The addition of the BST layer improved the 'battery' life of these electrochemical cells and also, increased the specific capacitance.

A thorough investigation of different methods to achieve an improvement in the electrochemical performance of the electrochemical cells was described. A mechanism for charge flow and sustenance was proposed that attempts to explain what causes or reduces the leakage in the electrochemical double-layer capacitor.

Dissertation Outline

Chapter 2 provides a thorough investigation of ferroelectric materials and Barium Strontium Titanate ($Ba_xSr_{1-x}TiO_3$) thin film's physical and electrical characteristics. A detailed description of BST's current applications is also discussed. The chapter also provides an in-depth explanation of tunability and its importance in BST films for high frequency and high power devices.

Chapter 3 provides the techniques used in the present investigation to deposit barium strontium titanate thin films for various applications. A detailed comparison, with advantages and disadvantages is illustrated.

Characterization tools used include Scanning electron microscopy (SEM), X-Ray Diffraction (XRD), Atomic Force Microscopy (AFM) and Transmission Electron Microscopy (TEM). A brief description of each characterization technique is discussed along with the results.

Chapter 4 provides details of the electrical characterization carried out on BST thin film samples. The methods of making these thin film samples (processing details) are also described in detail. Both DC and AC electrical characterizations were carried out on Semiconductor – Insulator – Metal structures. The chapter also describes the non-contact Corona-Kelvin Metrology, used for DC electrical measurements of BST thin films.

Chapters 5 and 6 provide a detailed description of the fabrication and characterization of using BST as a leakage barrier for G-PANI (graphene-polyaniline) electrochemical supercapacitor cells. The chapters provide details of Graphene-polyaniline electrochemical cells behavior in comparison to G-PANI+BST electrochemical cells. A mechanism model has been proposed to suggest the charge transport and leakage barrier. In chapter 5, the use of sputtering and electrophoretic methods for depositing a thin BST layer has been described and compared. In chapter 6, an approach of incorporating BST into a matrix-like structure with GPANI has been discussed. The electrochemical properties of these electrodes has been compared to standard GPANI electrochemical electrodes. The purpose of this study was to understand and improve the leakage characteristics of GPANI

electrodes using BST thin film layer to be used in supercapacitor applications.

Chapter 7 provides a brief overview of the results obtained in the previous chapters and correlates the experimental results. The chapter also presents new ideas for future work that can be implemented related to this field.

Chapter 2: Properties and Applications of Barium Strontium Titanate

Thin Films

Introduction

Use of very high efficiency communication devices has been the need of the hour for the past few decades. Cellular networks, smart computing, cloud computing, Bluetooth devices, high end military devices are just some of the applications. At the same time, improvements in global positioning satellite devices, satellite phones, smart phones, wireless devices has opened newer avenues for the communication technology. These technological advances have come to every household use. This has been possible due to the advancements in silicon technology and microfabrication. There is a huge research impetus into finding new solutions for improving communication devices [25, 26]. To improve the quality and reliable functioning of the end electronic products it is of utmost priority to thoroughly understand the properties of the materials that are used in the manufacturing of these products. Also, it is imperative to be able to manipulate the fundamental properties of these materials to 'tune' them to requirements. For example, the miniaturization of transistors was a crucial step in keeping up with 'Moore's law' but this was accomplished due to

advancements in understanding of high-k dielectrics and device geometries. Hence, to start with the understanding of ferroelectric materials, it is essential to understand their fundamental properties. This enables engineers to 'tweak' the end device properties.

What are Ferroelectric Materials?

Mechanical forces cause certain crystal materials to become electrically polarized [27]. The applied force generates voltages of opposite polarity, that is, the generated voltage opposes the mechanical strain. On the other hand, if an electric field is applied to the material, it deforms depending on the polarity of the field, which in turn is proportional to the strength of the field. These materials are categorized as piezoelectric and the behavior termed as piezoelectric effect. All crystalline materials are conventionally classified into 32 crystal classes of which 21 lack center of symmetry, which is an essential property required for the material to undergo piezoelectric effect. Out of the 21 crystal classes 20 show piezoelectricity. Out of the 20 there is a sub-group of 10 crystal classes which possess a unique polar axis. Due to this property this sub-group when uniformly heated generates an additional electric charge in addition to the piezoelectric effect related charge creation. This effect is termed as pyroelectric effect [28]. Some pyroelectric crystals possess a quality wherein upon applying external electric field the polarization of the crystals reverses over a range of certain temperature

range. This is observed as a hysteresis loop. These materials are termed as ferroelectric in nature [29-31].

Properties of Ferroelectrics

Ferroelectricity phenomenon was discovered as a result of Rochelle salt's ferroelectric properties in the year 1921 [32]. Later around the 1950s, great progress was made in the field due to the advent of other piezoelectric ceramics and man-made materials. It was established that the composition, shape and dimensions of a ceramic material can be tailored for a specific application to meet its requirements [19]. Over the past 30 years, ferroelectric ceramic materials have found applications as capacitors, thin films for non volatile memories, IR detectors, data storage, etc. [28]. Barium Titanate (BaTiO_3) was among the very first piezoelectric materials used in capacitor and piezoelectric transducer devices. Other ferroelectric materials like lead titanate (PbTiO_3), lead zirconate titanate (PZT), lead magnesium niobate (PMN) followed suite in being utilized for similar applications.

In the following sections, the uniqueness of the crystal structure, phase transition behavior and polarization of ferroelectric materials will be discussed in detail. This discussion is necessary to understand the fundamentals of ferroelectric materials behavior.

Crystal Structure of Ferroelectric Materials

Ferroelectric ceramic materials possess the same crystalline structure as that of the crystalline mineral CaTiO_3 , which is also termed as a perovskite. The structure can be described consisting of tetravalent metal ions (titanium or zirconium), in a lattice of large divalent metal ions (Barium or Strontium). The structure formed is called a perovskite ABO_3 structure and is represented in figure 1 [29]. The red atoms representing the metal ions located at the corners of the unit cell, green representing the relatively smaller titanium ions located at the body center and oxygen atoms located at the face center represented in blue. Symmetry is reduced in these structures due to distortions. This dis-symmetry is an effect of the displacement of the positive (due to barium or strontium ions) and negative (oxygen ions) with respect to each other, leading to a polar axis, in the direction of the deformation. This is a defining characteristic of ferroelectric materials which causes spontaneous polarization.

Many different perovskite structures can be formed by changing the cation (barium/strontium and titanium) sites, without drastically changing the overall structure of the basic material. A complete range of compositions is possible with different materials forming solid solutions.

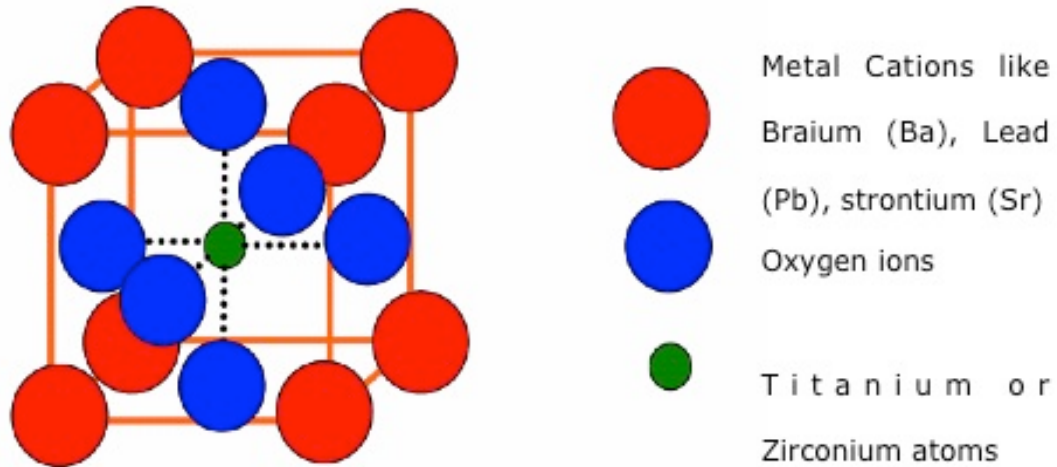


Figure 1. Crystal structure of typical perovskite material [29]

Properties of final structures, after mixing, are totally different from the basic individual metal ions due to the complexity of the interactions between them. Thus, even if two different cations are compatible in solution, their behavior can be radically different when apart from each other. This is the reason, why perovskite structures are popular, as their electronic, structural and dimensional properties can be tailored over a wide range depending on the end application. A detailed list of perovskite materials and their applications is given in table 1 [15].

Phase Transitions in Ferroelectric Materials

Ferroelectric materials are known to undergo a transformation from paraelectric to ferroelectric phase when cooled down below a certain temperature known as the Curie temperature (T_c), which is characteristic of each material. This property of phase change has been theoretically modeled using the Landau-Ginzburg-Devonshire (LGD) theory [31-33].

Table 1 Type of Perovskite materials and their applications [30]

Number	Type of Perovskite	Applications
1	Barium Strontium Titanate (BST)	Tunable devices, DRAM, IR imaging, high capacitance density decoupling capacitors
2	Lead Zirconate Titanate (PZT)	Thermistors, multiferroics, pressure sensors, acoustic sensor
3	Barium Titanate (BT)	Capacitors, acoustic transducers, microphones
4	Strontium Titanate (SrT)	Radioisotopic thermoelectric generator

Figure 2 represents the phase change and corresponding crystal structure change that leads to the phase transition [34]. The phase transition in perovskite ferroelectric crystals is due to the non centrosymmetric polar lattice (ferroelectric phase) and centrosymmetric non-polar lattice (paraelectric phase), below and above the Curie temperature, respectively. As shown in figure 2c, the dielectric constant increases with the increase in Curie temperature, whereas in the paraelectric phase, the

dielectric constant decreases with increase in temperature. This relationship is given by the Curie Weiss law [20], which is given as,

$$\epsilon_r = C/(T-T_0) \quad (2.1)$$

where ϵ_r is the dielectric permittivity, T_0 is the Curie-Weiss temperature (where T_0 is less than Curie temperature), T is the temperature where ϵ_r is being measured and C is the Curie constant.

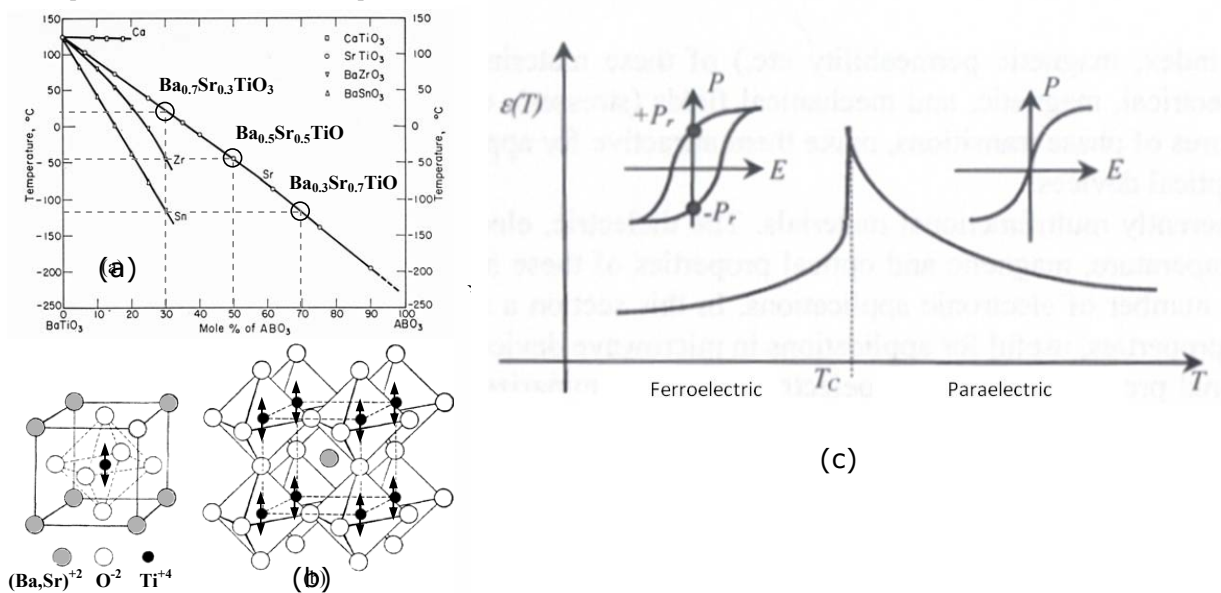


Figure 2. Electrical and physical properties of ferroelectric materials [35-36]

The tetravalent metal ion (Ti), below the Curie temperature, is in an off-center position leading to a permanent dipole. In this phase, the crystal structure changes to being tetragonal instead of cubic. Domains of particular alignment are formed between adjoining regions in ferroelectric phase. The alignment gives rise to a net dipole moment and hence a net polarization called spontaneous polarization. Since, the domain formation is due to stray

electric fields, which are non-compensated polarization charges, and are not aligned, there is no overall polarization unless an electric field is applied. Domains are separated by domain walls and stresses created at Curie temperature. They are also caused by physical imperfections (vacancies, dislocations and dopants). Ferroelectric materials possess hysteresis properties below Curie temperature. That is, when an electric field is applied to a ferroelectric material, the polarization increases due to alignment of dipoles of same polarity. When all dipoles of same polarity align, one gets maximum value of polarization which finally reaches saturated state. When the electric field is reduced from the saturation point, the polarization also reduces but it does not become zero. This is termed as the remnant polarization. Further down the electric field, reverse saturation point is reached, below which the polarization does not go any lower. The polarization characteristics of BST are illustrated in the inset of figure 2c [37]. This property of the ferroelectric material to 'remember' its last state, enables the use of these materials in non-volatile memory and piezoelectric applications.

In contrast, above the Curie temperature, due to thermal energy or applied electric field, it is possible to induce movement of the metal atoms (Ba, Sr) randomly from one point to another, so there is no fixed asymmetry. Upon application of an electric field, the octahedral site lets the tetravalent metal atom to develop a fairly large dipole moment. This is the

reason why perovskite ferroelectric materials possess high permittivity in paraelectric phase. In this phase, due to the high dielectric permittivity of the ferroelectric material, applications like that of frequency agile and microwave devices is possible.

Polarization and Dielectric Permittivity in Ferroelectrics

A ferroelectric material (in both phases) is considered a dielectric material. And polarization is a quantity which is used for defining the physical characteristics of all dielectrics. A microscopic and macroscopic view of the origin of polarization is described in the following section [38, 39].

A dipole is a system which consists of a positive and negative charge separated by a distance 'a'. The dipole moment is given by,

$$p = q \cdot a \quad (2.2)$$

where q is the charge of the particle. And the dipole moment for the system of charges is given by:

$$p = \sum q_i \cdot r_i \quad (2.3)$$

where 'r_i' is the position vector of the charges 'q_i'.

Polarization is defined as dipole moment per unit volume. Polarization of a dielectric material is due to the redistribution of charges inside the dielectric when an electric field is applied to it. At a macroscopic level there are no net charges present in the dielectric if no electric field is applied

because the dielectric has equal number of positive and negative charges. This fact is not true at the surface of the film since the charges are not compensated at the surface. Hence, for a polarizable dielectric, the charges appear near the surface producing electric field whose magnitude depends on these surface charges. The total electric field 'E' across a dielectric is given by,

$$E = E_0 + E_1 \quad (2.4)$$

where, E_0 is the applied field and E_1 is the field due to polarization of the solid. The field E_1 opposes the field E_0 and is called the depolarizing field. Figure 3 depicts the action of the depolarizing field. This field tried to break down the ferroelectric material into domains. 200V/mm to 500V/mm usually have a significant depolarizing effect [40].

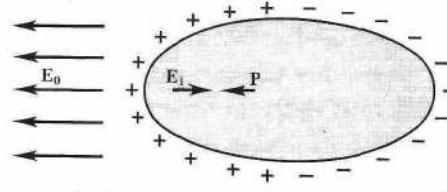


Figure 3. The depolarization field E_1 is opposite to P . The fictitious surface charges are indicated: the field of these charges is E_1 within the ellipsoid [40]

Mechanisms of Polarization in Ferroelectrics

Positive and negative charges are pulled apart under the influence of an electric field. This is the basic nature of all molecules. This property is termed as polarization. There are different types of polarization found in

dielectric behavior. The following section provides brief description on different polarization mechanisms [41, 42] –

1. Electronic Polarization: caused by displacement of negatively charges electrons from positively charges nucleus due to externally applied electric field.
2. Ionic Polarization: caused by stretching of ionic bonds in molecules of ionic crystals by displacement of ions. Change in ionic bond length induces a dipole moment.
3. Molecular Polarization: caused by the permanent moment, even in the absence of an external electric field. However, the net polarization of a dipolar material is zero in the absence of an electric field because the molecular moments are randomly oriented. Piezoelectric materials posses dipolar polarization.
4. Space charge: caused due to charge carriers in heterogeneous dielectric materials like BST. The charge carriers are accelerated due to an applied electric field until they are impeded by and pile up at physical barriers. Common barriers comprise of conducting grains, insulating grain boundaries and interfaces.
5. Orientation Polarization: described by the alignment of permanent dipoles in a material [41].
6. Domain Wall Polarization: occurs due to motion of domain walls that separates regions of differently oriented dipoles. Polarization takes

place by growth of domains which have similarly oriented dipoles with respect to applied field. Seen predominantly in dielectric response of ferroelectric materials.

Figure 4 [42] shows the different mechanisms that are discussed above with and without any external electric field. Types of polarizations are classified as extrinsic (electronic, ionic and dipolar) and intrinsic (space charge, orientation and domain wall) polarizations.

Polarization and dielectric permittivity are directly related to each other. And are expressed in terms of complex relative permittivity as

$$\epsilon_r^* = \epsilon' - j \epsilon'' \quad (2.5)$$

where, ϵ' is the real part of permittivity termed as dielectric constant which depends on the polarization magnitude. It gives the charge stored in a capacitor. ϵ'' is the loss factor and it represents the mathematical equivalent of all losses due to lag in polarization, energy dissipation and energy loss due to heat in a material. Another important quantity to consider is the loss tangent given by $\tan\delta$ and is given by,

$$\epsilon_r^* = \epsilon'(1 - j \tan\delta) \quad (2.6)$$

where, $\epsilon'' \tan\delta = \epsilon'$

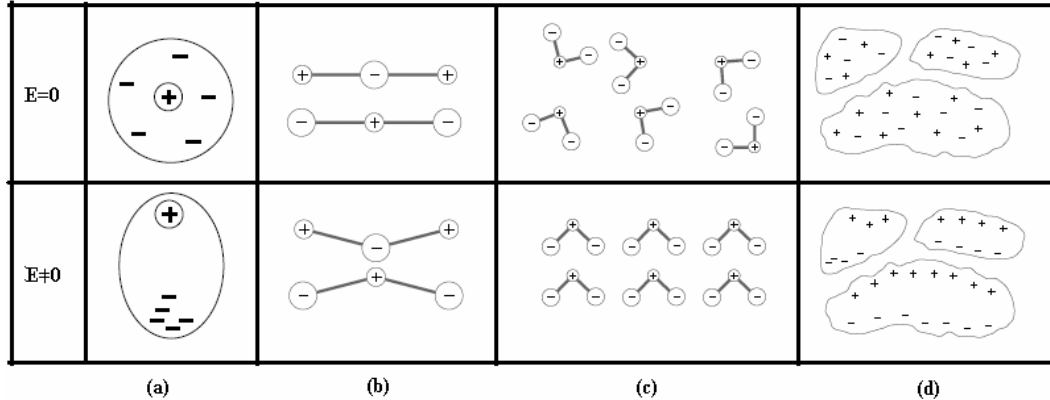


Figure 4. Polarization mechanisms a) electronic polarization, b) ionic polarization, c) dipolar polarization, d) space charge polarization [42]

Polarization and Frequency Response in Ferroelectrics

The frequency response of a dielectric material changes over different frequency ranges depending upon the different polarization mechanisms. This is due to the fact that polarization stems from minute moments of particles when an electric field is applied. Mass of a particle is the deciding factor for which mechanism comes into picture in producing the polarization. This can be explained using figure 5.

Here a_e , a_i and a_d stand for electronic, ionic and dipolar polarizations which correspond to ω_e , ω_i , ω_d frequencies respectively. At really high frequencies (above ultraviolet) the electronic contribution to polarization vanishes, above infrared, the polarization is due to electrons and below infrared, it is due to ionic molecules.

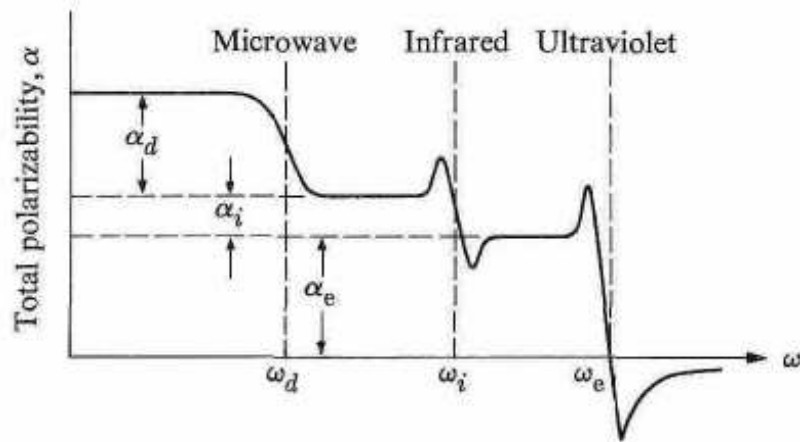


Figure 5. Frequency dependence of the several contributions to the polarizability [40]

Effect of Electric Field on the Behavior of Ferroelectric Materials

A strong electric field dependence on the permittivity of ferroelectric films opens their applications to a broad spectrum due to their nonlinearities. Applications include passive tunable capacitors, phase shifters, matching networks and filters. The ability to adjust the frequency tunability gives a design engineer an added advantage to tune multiple responses of the system.

Typical Capacitance-Voltage characteristics carried out on ferroelectric films at high frequencies yield a small AC ripple, which propagates through the film along with the applied DC bias. At first there is a slight increase in the permittivity of the films due to domain walls polarization effects but a further increase in the bias causes the domain walls to become immobile and the particle movement is constricted due to elastic constraints. So at high AC the dielectric response is due to the intrinsic contributions. [43-48].

Again when DC bias is reduced, the extrinsic contributions play a major role in influencing the dielectric behavior and the contributions reach a maximum at zero bias. At zero bias, or no electric field, maximum permittivity is attained accompanied by maximum losses (as described in previous sections). Conversely, at maximum bias, minimum permittivity and losses are observed in these ferroelectric films. Thus, a bell-shaped curve is observed with a sweep from minimum to maximum driving of the voltage applied [44].

In the ferroelectric phase, a “butterfly loop” is obtained with two distinct peaks in capacitance values whereas in the paraelectric phase, a “bell shaped” curve with no “butterfly loop” is observed. The “butterfly loop” is due to the presence of hysteresis in the ferroelectric phase, which is clearly absent in the paraelectric phase. Figure 6 shows the typical CV characteristics of ferroelectric films in ferroelectric and paraelectric phase [18].

Tunability defined at high frequencies is a very important property of ferroelectric films. This is due to the high spectrum of frequency agile applications these ferroelectric films are used. The tunability can be expressed in terms of the relative dielectric permittivity as follows

$$n (\%) = \{ \epsilon_r (\max) - \epsilon_r (\min) / \epsilon_r (\min) \} * 100 \quad (2.7)$$

where, n represents the tunability and ϵ_r (max) and ϵ_r (min) are the maximum and minimum permittivities at applied electric field. There is a trade-off between the tunability and the loss tangent.

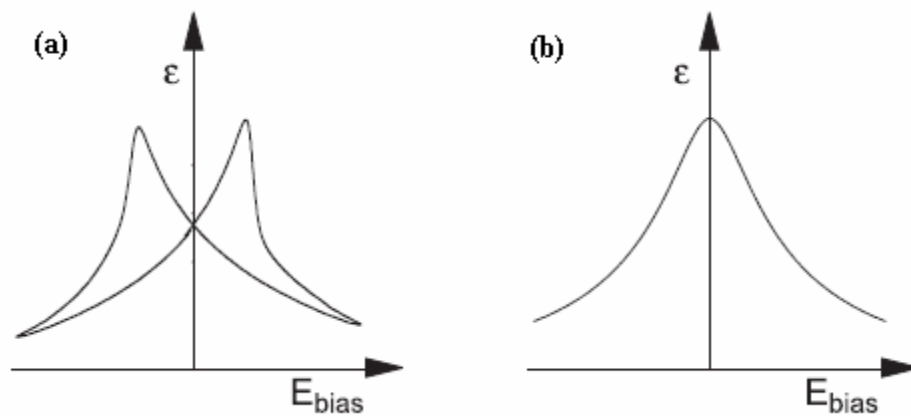


Figure 6. Variation of permittivity with applied bias for a ferroelectric material in a) ferroelectric phase and b) paraelectric phase [18]

Microwave applications make use of the paraelectric phase tunability and loss tangent and hence, large electric fields have to be applied to achieve these values. Nominal values of electric field are of the order of 1000KV/cm [49, 50].

The following sections provide a brief description of the ferroelectric dielectric properties of Barium Strontium Titanate with respect to the preceding sections.

Material Properties of Barium Strontium Titanate (BST)

Barium Strontium Titanate ($\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$; BST) is a continuous solid solution ferroelectric between Barium Titanate (BaTiO_3) and Strontium Titanate (SrTiO_3). The Curie temperature of BST can be manipulated by changing the ratio of Ba to Sr at the rate of 3.4°C per mole of %Sr. Since the Curie temperature is manipulative, the properties of BST can be tailored to meet a whole range of applications [51]. Conventional ferroelectrics lack this flexibility in property manipulation. Hence, BST poses an edge over conventional ferroelectrics and meets a wide range of applications. Figure 7 gives an illustration of the application areas in which BST is used.

Crystal Structure of Barium Strontium Titanate (BST)

BST belongs to the ABO_3 perovskite family and possesses the similar crystalline properties as that of general perovskites. It can exist in both cubic and tetragonal crystal symmetry which depends on the (Ba to Sr) ratio and corresponding Curie temperature. The ABO_3 structure comprises of the Ba^{2+} and Sr^{2+} atoms occupying the corner positions. This gives rise to 0.5 Ba and 0.5 Sr shared atoms per unit cell. The 6 oxygen atoms take the face centered position and hence there are 3 oxygen atoms per unit cell. The Ti^{4+} atom in the crystal is located at the center of the cubic cell which is the main constituent causing the spontaneous polarization of BST [52]. The crystal structure of BST has been illustrated in the preceding section, in figure 1.

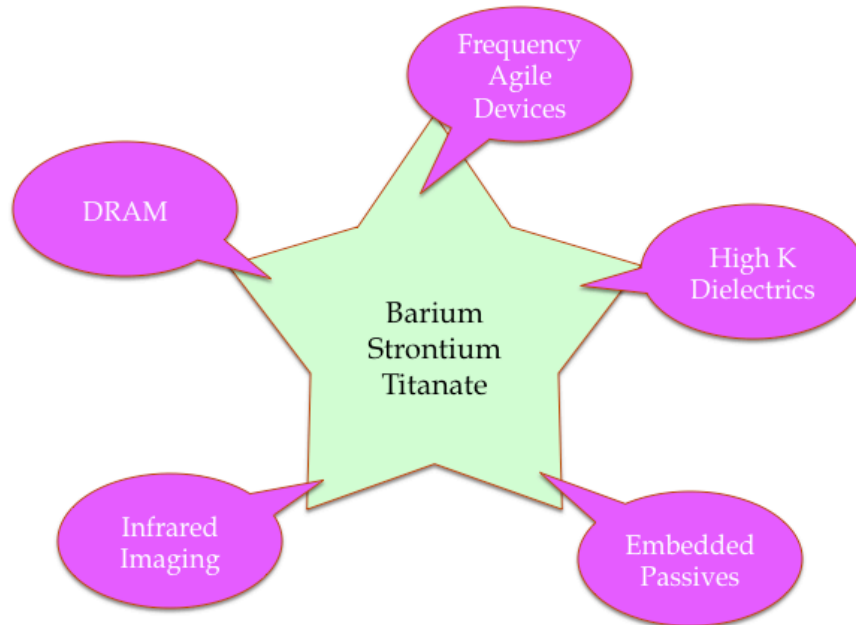


Figure 7. Applications of BST thin films

Phase Transitions in BST

Figure 8 gives the relationship between the barium concentration, cubic lattice parameters and Curie temperature (in Kelvin).

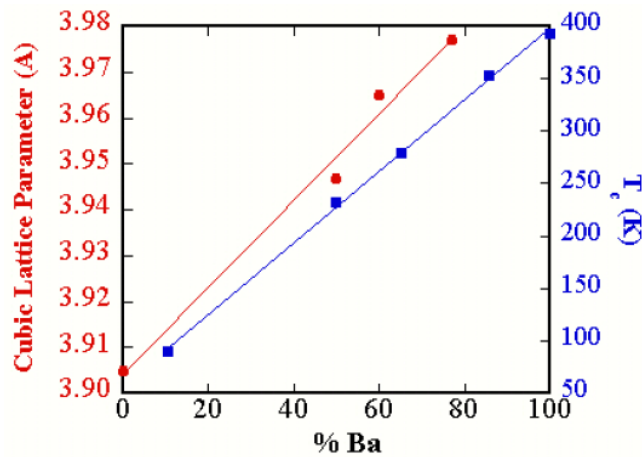


Figure 8. Relationship between barium mole concentration (%), cubic lattice parameter and Curie temperature (K) [53]

It is evident from the graph that the phase transition behavior of BST evolves with the composition. Barium Titanate (BaTiO_3) undergoes phase transitions as it goes from being a ferroelectric to paraelectric material. Strontium Titanate (SrTiO_3), on the other hand, exhibits a much lower temperature phase transition which is way below its Curie temperature. This is due to quantum ferroelectric effects in SrTiO_3 [54]. BST undergoes structural as well as phase transitions for changing Ba and Sr % concentrations. As the concentration approaches that of pure SrTiO_3 , there is a competition between prototype ferroelectric transitions and quantum transitions related instabilities. It has been shown in previous reports [55] that a concentration of barium to strontium of around 0.5 is ideal for room temperature tunable microwave applications. This is due to the fact that the phase transitions in BST take place below the room temperature.

Thickness also plays an important role in the variation of the dielectric constant at room temperature. This is evident from figure 9 [56].

The origin of the variation of the phase transition and thickness with respect to the Curie temperature has still not been well understood [57]. The effect of changing the substrate on the Curie temperature has been reported [53]. It has been shown that the Curie temperature increases due to the internal stresses developed in the film and a difference between the thermal coefficients of expansion (TEC) or the difference in the lattice parameters between the film and the substrates [58, 52].

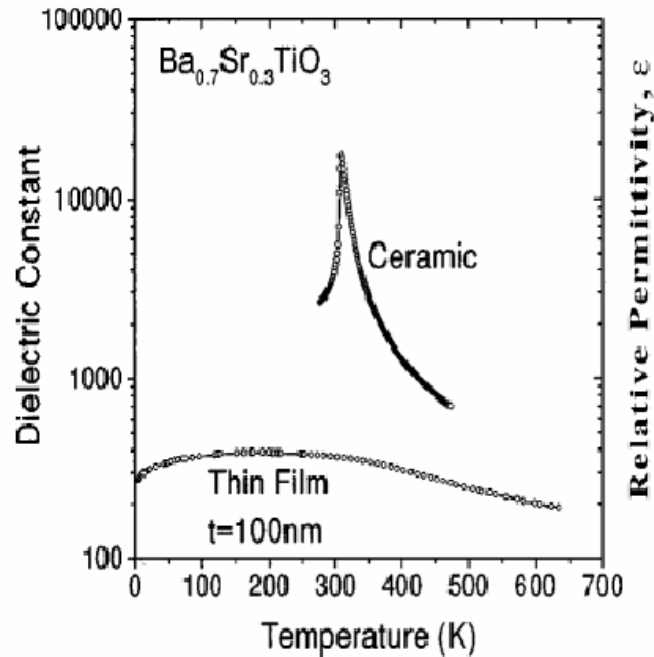


Figure 9. Comparison of variation of dielectric constant with temperature between ceramic and thin film BST [52]

The hysteresis behavior of BST thin films is illustrated in figure 10. It can be seen from the figure that less than 70% concentration of Barium in BST thin films, gives rise to very little hysteresis.

Polarization Mechanism in BST

Previous reports have suggested that, “near the surface of a ferroelectric thin film, the polarization normal to the surface should continuously decrease from the bulk value” [60]. It has been noted that, at the surface, the polarization is reduced as compared to the bulk, thus reducing the overall capacitance of the film. This is due to the formation of a “dead layer” due to suppression of ionic contributions [61].

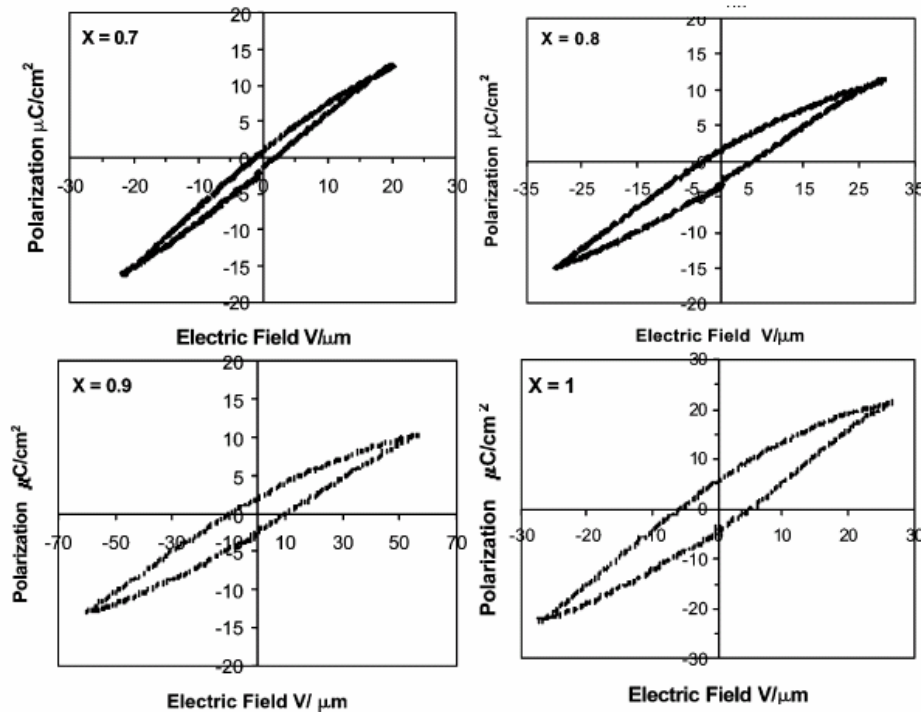


Figure 10. P-E hysteresis loops for BST thin films at room temperature [59]

Stresses developed in a BST thin film during growth, lattice mismatches and thermal expansion mismatch stresses can also affect the domain structure [62]. Both tensile and compressive stresses can be developed in BST thin films which can lead to pulling of the polarization into the plane of the film or directing it normal to the surface. Tensile stress can give rise to high dielectric constant whereas compressive stress leads to low dielectric constants [63-67]. For thin film applications being used in paraelectric phase, stresses do not come into picture.

Microstructure and Point Defect Chemistry in BST

The microstructure of BST thin films has known to play a very crucial role in the electrical properties of the devices. Hence, it is very essential to study and understand the relation between the microstructure and film properties of the thin film [62, 68].

York et al [34] have reported that (100) orientation in BST thin films is preferred and leads to smoother films, which in turn, leads to better film properties. The substrate tends to affect the crystallinity of the films as well. Silicon substrates usually lead to polycrystalline films, ceramic substrates like Al_2O_3 and MgO are known to form single crystal epitaxial BST thin films [69].

Lower grain size (less than $1 \mu\text{m}$) causes low permittivity layer in grain boundaries and thus slowly decreases the dielectric permittivity. It has been shown by Adikary et al. [55] and Shaw et al. [58] that strontium content is inversely proportional to the grain size, so as the strontium content increases, the grain size decreases, thus, decreasing the dielectric permittivity.

The grain boundaries play a major role in decreasing the dielectric permittivity in BST polycrystalline films. Another factor that has a strong connection with the dielectric permittivity is the barium+strontium ratio with titanium (Ti). It has been shown [69] that the highest value of dielectric

constant is achieved when the ratio is equal to unity and excess Ti causes the relative permittivity to decrease monotonically. A columnar structure has shown to have negligible effect on the overall permittivity of the films since the grain boundaries lie perpendicular to the electrode. There is a marked effect on the permittivity due to the grains in the grainy films lying parallel to the electrode [62].

Frequency Response in BST

At low frequencies, the capacitance of BST in the paraelectric phase decreases with the applied bias. The decrease in permittivity has been explained in the earlier sections. Typical capacitance-frequency curves for $\text{Ba}_{0.5}\text{Sr}_{0.5}\text{TiO}_3$ thin films are shown in figure 11 [70].

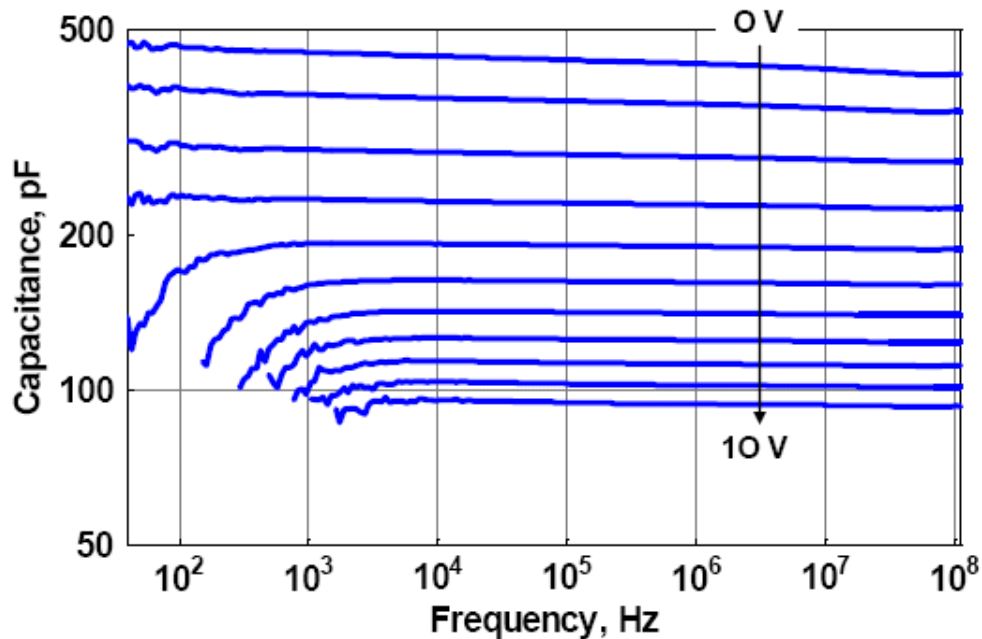


Figure 11. Typical capacitance-frequency response for BST thin films [70]

At higher frequencies, the 'field-induced piezoelectricity' of the material phenomenon comes into the picture [70], which, has been explained by electrostriction phenomenon. It is an electromechanical coupling mechanism which occurs in centro-symmetric crystals. It can be defined as the strain developed in a material and the electric field applied to the film and it is known to be tunable, reproducible and non hysteretic [52, 71].

This resonance which comes into picture for BST thin films has an adverse effect on the losses of the device. Hence, a thorough understanding of these resonances to obtain reliable capacitors for microwave and other frequency tunable applications is very essential [52, 71]. Figure 12 shows the bias-induced resonant dips observed in BST-based MIM capacitor with increasing bias values [73].

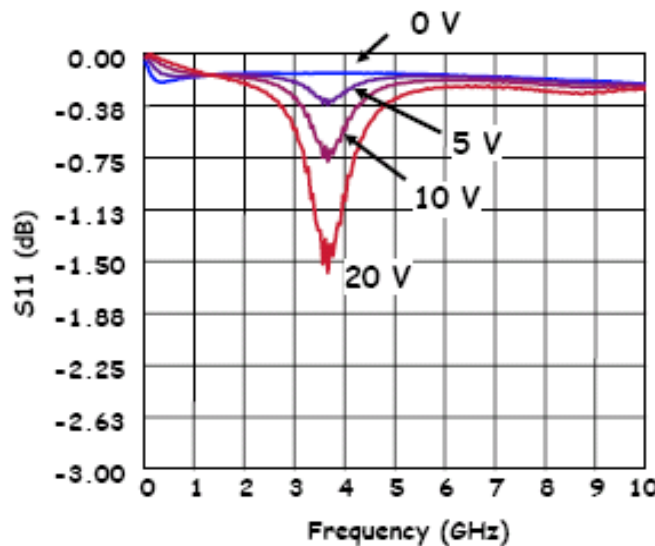


Figure 12. Bias-induced resonant dips observed in BST-based MIM capacitor with increasing bias voltage [73]

Resistance degradation has been reported to be a huge concern in BST thin films [74-76]. Resistance degradation is calculated by measuring the time required for the leakage current density to increase by an order of magnitude from its steady state value. Waser et al [41] have suggested that it occurs due to the migration of charges oxygen vacancies.

Need for Tunable Devices

The use of semiconductor diode varactors has been prevalent for many decades now [60]. Various frequency tunable devices that have been made and studied include varactors, varactor circuits, tunable filters, phase-shifters, linearization networks, voltage controlled oscillators, etc. Even though the tuning mechanism is different for tuning diode varactors and dielectric varactors, they have shown to have similar tuning ratios and quality-factors. One of the key advantages of dielectric varactors is that they do not have forward conduction region and hence are known to sustain large RF voltage swings [20]. Another known advantage of dielectric varactors is their ease of fabrication for the same quality factor Q and hence can be easily integrated with integrated silicon circuits. This leads to an economically attractive solution. Whereas, diode varactor integration is well established in silicon fabrication technology. Therefore, dielectric varactors have found uses in front end communication device technology. Thin film BST has been previously used as high density capacitance decoupling capacitor material [61-64]. In the last decade the attention has shifted to

fabricate frequency tunable capacitors. The present investigation is an attempt to find a viable solution in this direction by understanding the leakage behavior of BST thin films using simple MIM structures deposited on silicon, platinized silicon and ceramic substrates.

Chapter 3: Deposition and Physical Characterization of Barium

Strontium Titanate Thin Films

Factors Affecting BST Thin Film Properties

The quality of BST thin film plays a very crucial role in its electrical properties. Various deposition methods can be used to deposit thin films of Barium strontium titanate (BST) with different stoichiometries. The methods which are popularly used are RF magnetron sputtering, pulse laser deposition (PLD), metal organic chemical vapor deposition (MOCVD) and sol-gel (which is a drop-casting or spin-on method) [65-68]. To have better compatibility with other CMOS processes, it is essential to have the lowest possible process temperature. Post-processing annealing temperatures and oxygen pressures also have to be maintained in a range where the resistance of the thin films is not affected because of the change in stoichiometry. The advantages and disadvantages of different deposition methods have been summarized in table 2 [21, 70].

Thus, MOCVD and sputtering are good for mass production and sol-gel is good if a fast and inexpensive method. For the present work, RF magnetron sputtering and sol-gel process have been chosen to deposit BST thin films. Also, the stoichiometry for the target film was decided to be

$Ba_{0.6}Sr_{0.4}TiO_4$ for it is high dielectric permittivity, room temperature paraelectric phase behavior and dielectric tunability.

Table 2 Comparative table of BST thin film deposition methods [21, 70]

Method	Advantages	Disadvantages
RF magnetron sputtering	Uniformity, Scalability, Low growth Temperature, Standard IC Processing	<ul style="list-style-type: none"> • Residual Stresses • Point defect concentration
Sol-gel	Inexpensive, low capital investment Rapid sampling of materials Quickly produce new materials	<ul style="list-style-type: none"> • Phase control • Composition Control • Morphology Scalability
Pulsed Laser Deposition	Non-equilibrium deposition Highly stoichiometric films Quickly produce new materials	<ul style="list-style-type: none"> • Particulate formation • Uniformity • Morphology
MOCVD	Uniformity, Morphology, composition control	<ul style="list-style-type: none"> • Expensive • Precursor availability stability

Film Composition of BST Thin Films

Ratio between (Ba+Sr) and Ti is a major deciding factor for the dielectric constant [71]. T.Kawahara et.al [72] have suggested that a (Ba+Sr) to Ti ratio of 1:1 yields highest dielectric constant at room temperature. Also, as the Sr content is decreased it increases the dielectric constant. It has been also shown [73-75] that BST thin films which have compositional grading have higher dielectric constants as compared to uniform film composition. Maximum tunability has been reported for (Ba+Sr)

to Ti ratio of 0.93 [76]. There is a trade off between tunability and quality factor when Ti's percentage is increased beyond a certain limit.

Microstructure of BST Thin Films

The grain size of the films is another important aspect to be considered. It has been shown by G. Arlt et. al [79] that as the thickness of the film decreases, it increases the grain size and the grain boundaries, thus, worsening the leakage current. Increased dielectric constant and is possible with thicker films [80].

Crystalline Structure of BST Thin Films

High in-situ deposition temperatures lead to poor crystallinity and higher leakage currents [71]. Hence, for films in this present investigation, the in-situ growth temperature was maintained at 400°C. Different types substrates also play an important role in the crystallinity of the films and hence the dielectric constant. For example, Pt-coated substrates have been studied extensively, and require a lower deposition temperature because of Pt/Si interdiffusion problems [72]. Post-deposition high temperature (600 – 900°C) and long duration (9-12hrs) anneals tend to re-crystallize the films and improve the texture of the films which, in turn, leads to better tunability in processed thin films of BST [76].

Surface Morphology of BST Thin Films

It has been shown [77], that as the O₂ to Ar ratio of carrier gases is changed, the surface roughness of the films increases because of the shorter mean free path available for the Ar atoms, which affects the leakage of the deposited thin films. Another factor which controls the surface morphology of the films, is the substrate. It has been shown before that the deposited BST thin film 'mimics' the surface morphology of the substrate.

Film Thickness of the BST Thin Films

The thickness dependence of dielectric constant and permittivity in BST thin films has been explained using the Schottky barrier model by C. Basceri et al. [82] and Feng Yan et al. [83]. It has been shown that, the dielectric constant decreased with decrease in thickness of BST thin film.

The following sections give a brief description of the different BST deposition methods we have adopted for the present work and their advantages and disadvantages. Different analytical tools that were used during this work and their significance has also been explained in detail.

Deposition of BST Thin Films

RF Magnetron Sputtering

Figure 13 shows the Kurt J Lesker model CMS - 18 RF magnetron sputtering system available at USF. The operation of a RF magnetron sputtering system is explained in detail in Appendix B.

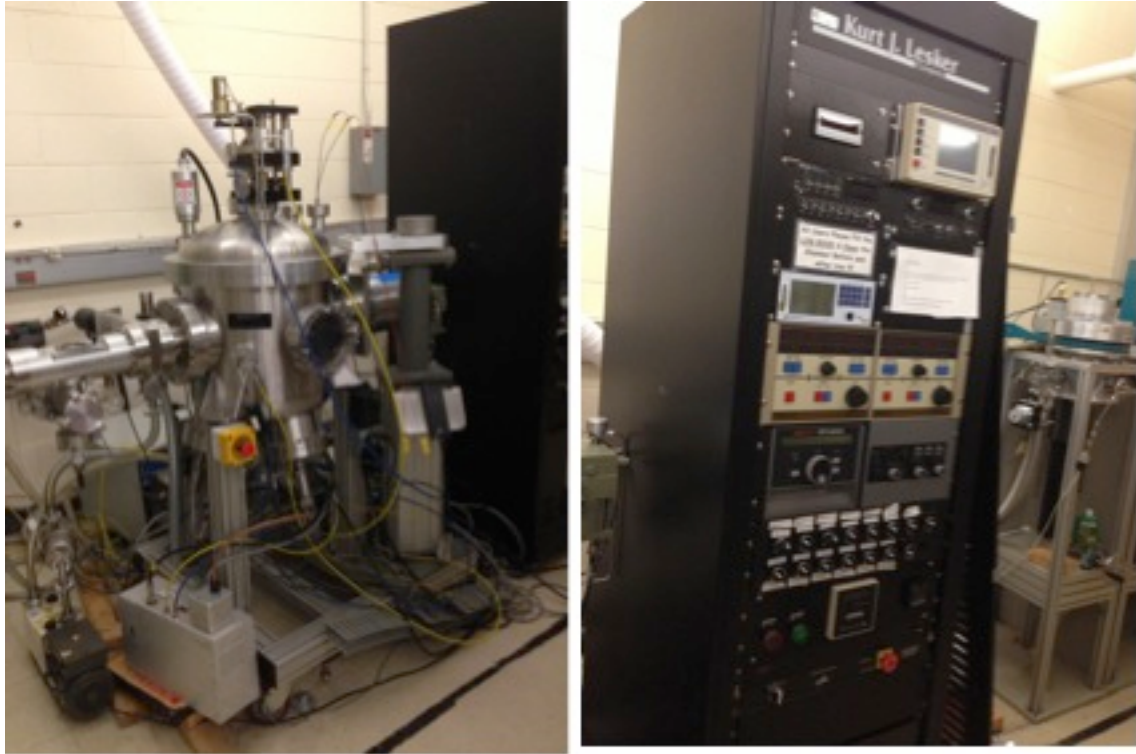


Figure 13. CMS - 18 Kurt J Lesker RF magnetron sputtering system

$Ba_{0.6}Sr_{0.4}TiO_3$ target stoichiometry was chosen for deposition of films. A 3" target is used in the standard Kurt J Lesker system purchased from a vendor as a starting material. The CMS-18 Kurt J Lesker is a thin film deposition system for advanced research and development environment. It has 3 Taurus magnetron sputtering deposition guns and a capability of hooking up these guns to either 2, DC or 1, RF power source which can go upto 600W. It can accommodate upto 6" wafers at a time. The system has a 4 speed changeable motor to spin the wafer at a constant speed during deposition to ensure uniform deposition. The chamber has 1 viewing port for in process inspection. An IR lamp is provided just above the wafer holder

assembly in the system's lid for in-situ sample annealing that can heat the wafer to upto 600°C. A mechanical vacuum pump which is capable of pumping the 18" diameter chamber to less than 50mT is attached for low vacuum requirements and a cryopump for high vacuum regime. An attached helium compressor to the cryopump ensures it is proper functioning.

The system was pumped down to 2×10^{-7} Torr to ensure as high vacuum as possible and improve the deposition speed and quality. Four different types of substrates were used during the work and their properties compared, viz., silicon (n and p-type), Platinized silicon (further referred to as Pt-si), Alumina (Al_2O_3) and sapphire. To optimize the growth conditions like rate, partial deposition pressure and distance between the target and the substrate, 6" silicon wafers were chosen. Table 3 shows the list of deposition parameters used for our BST thin films. The starting values for deposition conditions were gathered from literature and then optimized in order to achieve the best possible growth rates and film coverage.

Figure 14 (a-c) displays the deposited BST thin films. These films were deposited with different target to substrate distance and different base pressure. It can be seen that as the distance between the substrate and target is reduced, the coverage of the film deposited increases from 3.5" to almost 5.5".

Table 3 BST thin film deposition conditions

Deposition Parameters	Values
Substrate Temperature	400°C
RF power	200 W
Total pressure	25 mTorr
Ar/O ₂ ratio	90/10 sccm
BST thickness	280 nm
Deposition time	10 hours
Growth rate	28 nm/hour
Distance between the target and substrate	8cm

The color of the oxide also changes indicating a higher deposited thickness. Table 4 shows the thickness measurements taken across the wafer. The time of deposition was kept same, so it also suggests increase in deposition rate.

A detailed discussion for the above wafers is as follows:

1. For the wafer depicted in figure 14a, the BST deposition was observed to be uniform within 3.5"-4" diameter. The different colored circles indicate a non-uniform BST thickness around the periphery of the inner blue circle. The boundaries of the circles were muggy and had a smoky look.

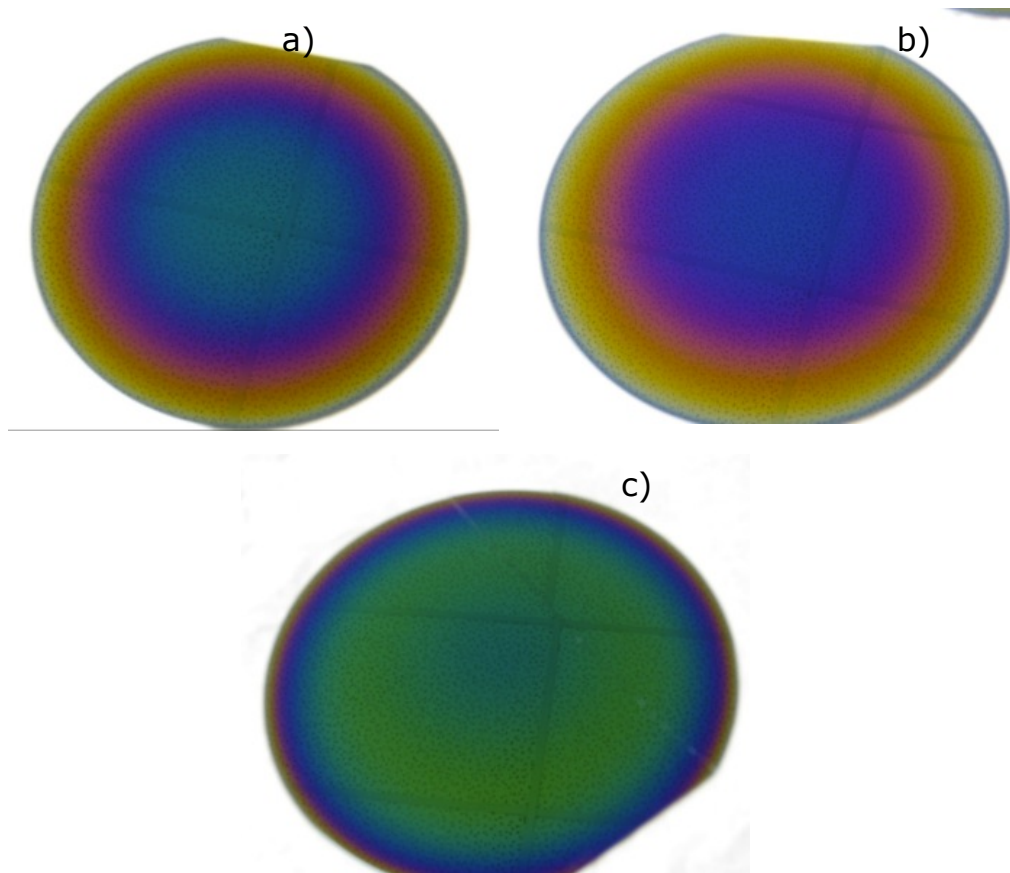


Figure 14. a), b) and c) RF magnetron sputtered BST thin film wafers

Table 4. Thickness profile data for different wafers

Wafer #	Maximum thickness in nm	Minimum thickness in nm	Standard deviation	Uniformity
1	239	158	25	1.61
2	240	190	12.4	2
3	294	207	21.4	2

- For the wafer shown in figure 14b the deposition was much better than that observed with a base pressure in the microTorr range. The film colors were brilliant.

3. For the wafer seen in figure 14c, the deposition was the best among three depositions with respect to the coverage (~5"-5.5"). It had a better color over that with condition (a). The film colors were brilliant.

Sol-gel Drop Casting

Sol-gel drop casting is a simple process in which, the material to be deposited is dissolved in a polymeric or acidic medium in a liquid form and then sprayed on to the substrate. Once a uniform thin film is sprayed and spun on the substrate, the substrate is annealed at high temperatures (depending on the solvent's evaporation temperature) to evaporate the solvent. The functional material then solidifies and then crystallizes to form thin films. It is a common method to pattern semiconductor devices, in photolithography [86, 87]. This method gives the flexibility of depositing very thin – monolayers of molecules of functional material to tens of micrometers.

The stages of sol-gel solidification can be described as follows –

- A diphasic gel-like system evolves from the solution whose morphology ranges from discrete to particles to continuous polymer networks. Sometimes, when the solvent content is very high, a significant amount of liquid needs to be removed for the gel-like properties to be revealed. Sedimentation or centrifugation can be employed to get rid of the excess liquid.

- Drying process causes shrinkage and densification. The rate at which drying can be carried out is determined by the required porosity of the film, since the microstructure of the final component determines the properties of the film.
- A final step of sintering or firing the sample is necessary for densification and grain growth of the films. An advantage of this process of densification is achieved at a lower temperature than other similar film deposition processes [80].

In this case, the sol-gel process was chosen for the following reasons-

- Ease of manipulating BST stoichiometries
- Comparative study and understanding of chemical interactions in BST
- Economical and low-temperature approach
- Thickness variation possible with very little effort
- Time to deposit BST thin films lesser than sputtering

Figure 15 adopted from [88] illustrates how the deposition is carried out during the drop casting process. Sol-gel films of target stoichiometry $Ba_{0.6}Sr_{0.4}TiO_3$ were spin coated on silicon and Pt coated silicon substrates and annealed at temperatures 600 or 700 or 800 °C to study the leakage current behavior corresponding to the crystal structure of these films.

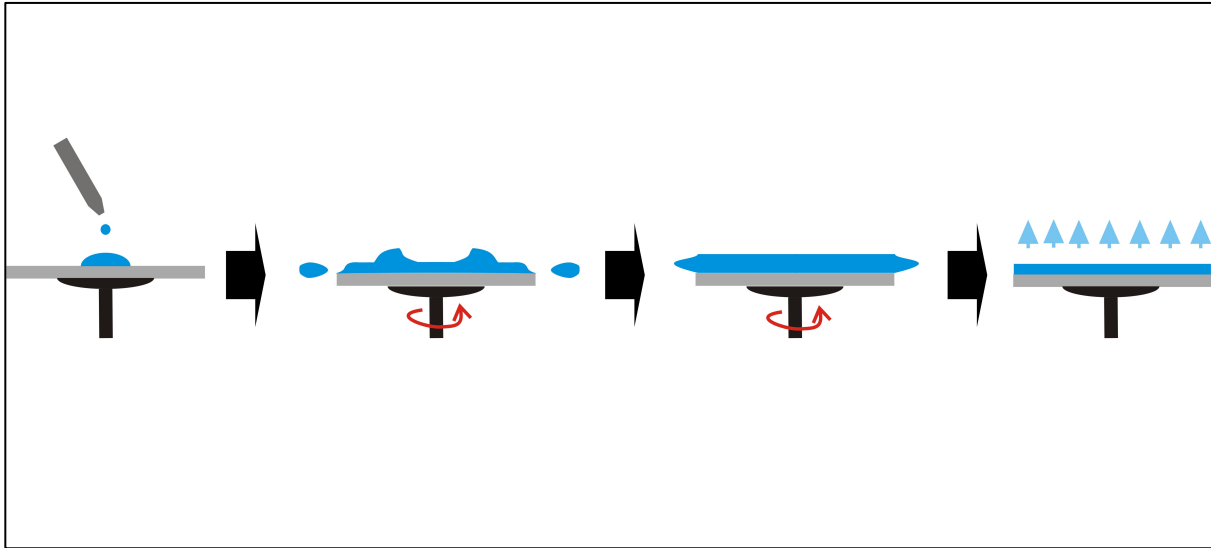


Figure 15. Spin coating process [100]

Figure 16 shows the flow diagram of the sol-gel synthesis of BST gel used for depositing thin films in the present study. The multicomponent BST sol was synthesized using barium (Ba) and strontium (Sr) acetates (99.5% in isopropanol, Aldrich), and titanium (Ti)-isopropoxide (99.999%, Aldrich) as starting precursors. 20 μ l of ethylene glycol was added to 20 ml of the prepared sol-gel as a surface modifier. Details of this sol-gel preparation are given in Appendix C.

After the BST sol was prepared, it was refrigerated at all times. The substrates were spin coated with a drop of 1ml of the prepared BST sol at a speed of 2400 rpm for 45sec. One or multiple consecutive spins were used for spin coating the samples. After spinning, the samples were baked at 150 $^{\circ}$ C for 1 min to evaporate the organics. The annealing was carried out in

a quartz tube furnace in air ambient for 1 or 5 hours and the change in the XRD patterns were studied.

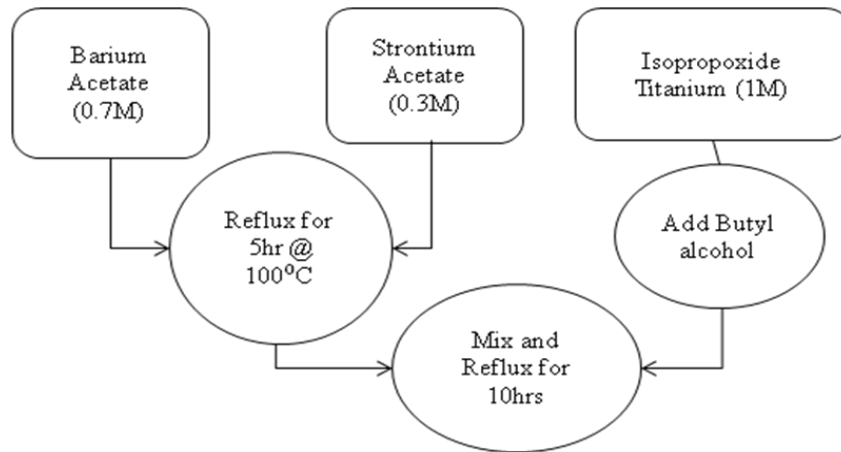


Figure 16. BST sol-gel preparation flow-chart

Stack Deposition

Figure 17 shows the 'Stacking' deposition process. The sputtering and sol-gel processes are as described before.

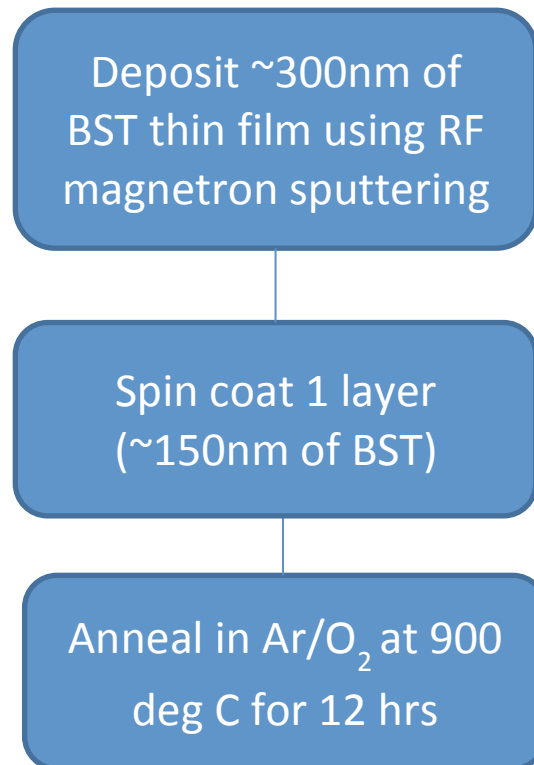


Figure 17. Flow diagram of 'stack' thin film BST deposition.

Annealing

Figure 18 shows the table top furnace used for annealing which has a programmable temperature microcontroller and a gas flow controller with gas lines for oxygen and nitrogen. Annealing was performed on both types of samples, for different times (4, 6, 9 and 12 hrs) and two different durations (600 and 900°C).

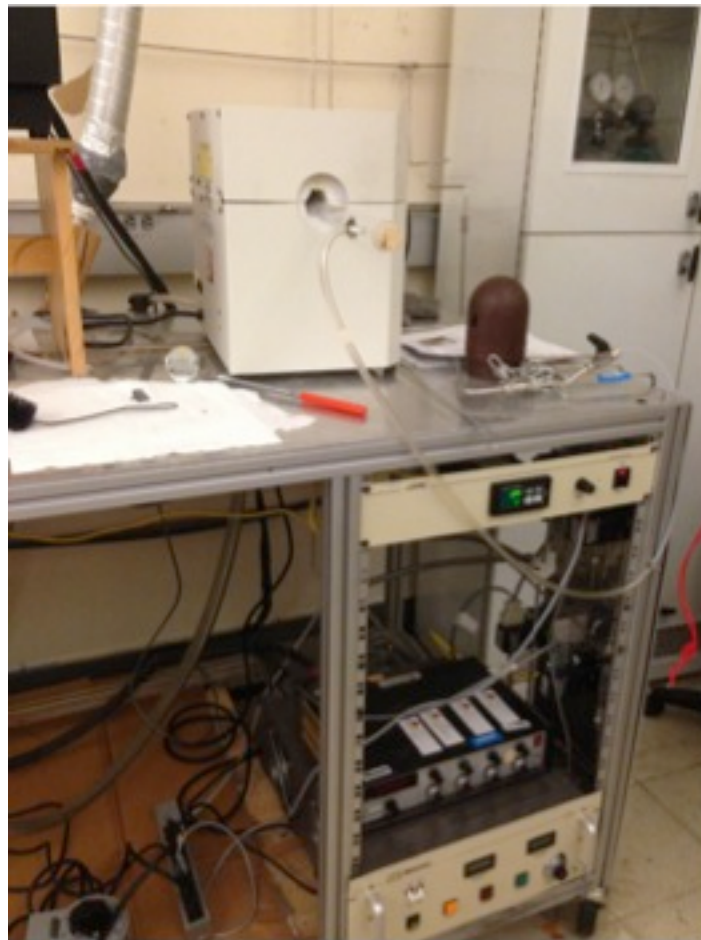


Figure 18. Table top furnace used for BST thin film annealing

Analytical Characterization of BST Thin Films

The thickness of the deposited films was measured using a Dektak Veeco 7M profilometer after etching. The films were structurally characterized by X-ray diffraction (XRD), atomic force microscope (AFM; Model – DI Nanoscope 5.12), Scanning electron microscopy (SEM; HITACHI S-800) and Transmission electron microscopy (TEM; Tecnai F20).

Ni-filtered Cu K α radiation with a detector slit size of 1 $^\circ$, slit height of about 2 mm, and step size of 0.02 $^\circ$ was used to determine the texture of the BST films by XRD (Philips Xpert x-ray diffractometer). The electrical measurements were performed using an HP 4284 LCR meter and the corona-Kelvin metrology tool instrumentation (FaaST Tools, SemiLab-SDI).

Thickness Measurement of BST Thin Films

The bulk thickness measurement of the sputter deposited samples yielded the thickness range of 240 to 295nm for a deposition period of 10hrs at the conditions stated earlier. It was observed that the thickness outside a diameter of 89 mm reduced to 60% of the center thickness at a distance of more than 203 mm between the target and the substrate. This distance was later changed from 203 mm to 89 mm by moving the target towards the rotating wafer. After this change the diameter of uniform deposition increased to 127 mm on a 152 mm wafer. This marked improvement in the deposition area could be employed to achieve confidence in device reliability and yield. The samples that were spin-coated using sol-gel BST technique

had a thickness of $\sim 125\text{nm}$ after just one spin-coating and a thickness of $\sim 270\text{nm}$ after 2 subsequent spin-coats.

Bar graph (figure 19) gives a detailed comparison and summary of thicknesses achieved using the 3 different techniques to deposit BST thin films. It can be seen that different conditions in sputtering correspond to 3 types of deposition recipes followed (different temperature, time and gas flow). For sol-gel process the 3 different bars respond to 3 layers of spin coating. And for 'stack' deposition, it is the combination of the best rate of sputtering and 2 layers of sol-gel deposition. A progressive thickness growth is observed in these samples.

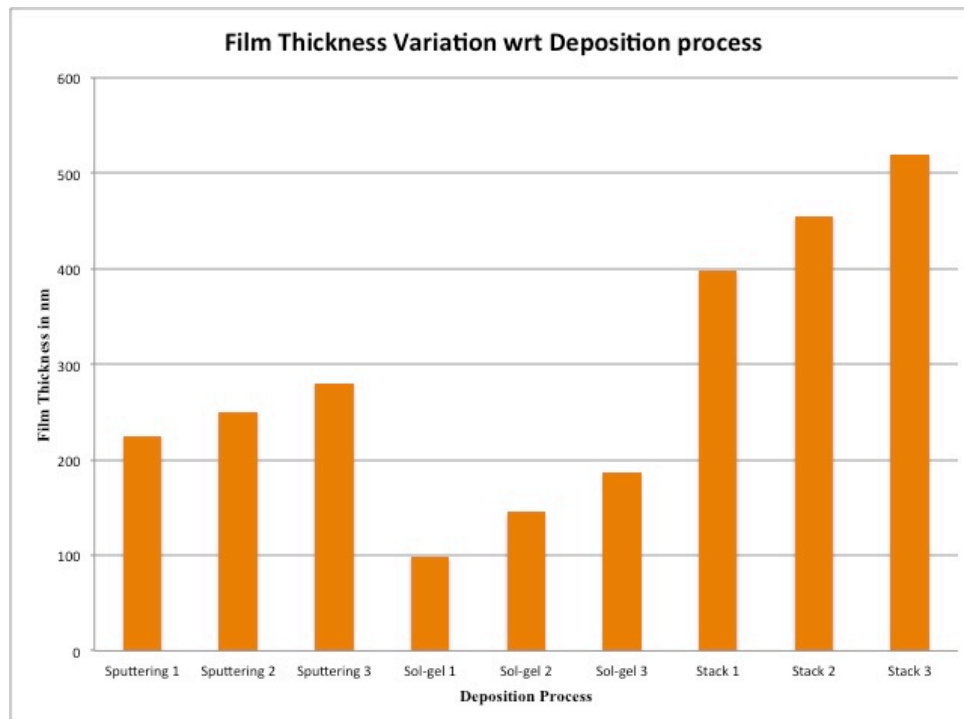


Figure 19. Progress in thickness control over deposition development.

Structural Results Using XRD Technique

X-ray diffraction (XRD) is a simple, widely used versatile tool which is used for studying the crystal properties of thin films. The properties that can be studied using XRD include – detection and confirmation of unknown material, matching lattice constants, understanding the crystal orientation (of polycrystalline and single crystalline films), particle size, etc. XRD is a non-destructive method which does not require elaborate sample preparation [89]. The basic principle behind the use of XRD can be defined by Bragg's law which is given as,

$$n\lambda = 2d\sin\theta \quad (3.1)$$

where, n is a positive integer representing the order of diffraction peak, λ is the X-ray wavelength, d is the distance between the plane of atoms and θ is the angle of incidence of the X-rays. Figure 20 shows the schematic of the working principle.

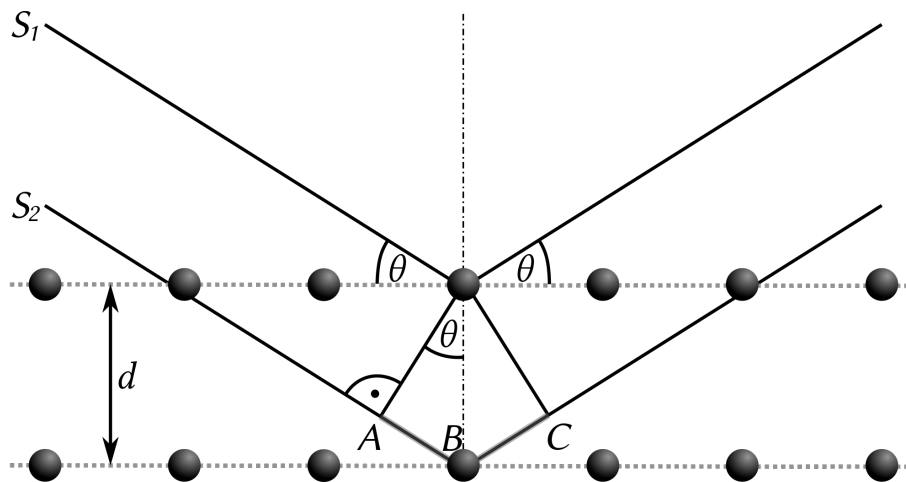


Figure 20. Illustration of Bragg's law [103]

S_1 , X-ray beam impinges the crystal surface at an angle θ and gets reflected from the atoms plane which are represented by black balls. A similar X-ray beam, S_2 also gets reflected from a parallel plane of atoms. The two reflected X-ray beams travel different distance which is given by $\sin\theta$. S_1 and S_2 reflected beams have a integral phase difference because they travel a different path. A constructive interference of the reflected rays occurs when the path difference between the ways is an integral multiple of the wavelength. The resultant reflected waves form a 'characteristic' diffraction pattern which is plotted as intensity (Intensity or Arbitrary Unit) vs 2θ graphs. This pattern is compared to known database which is specific to each material.

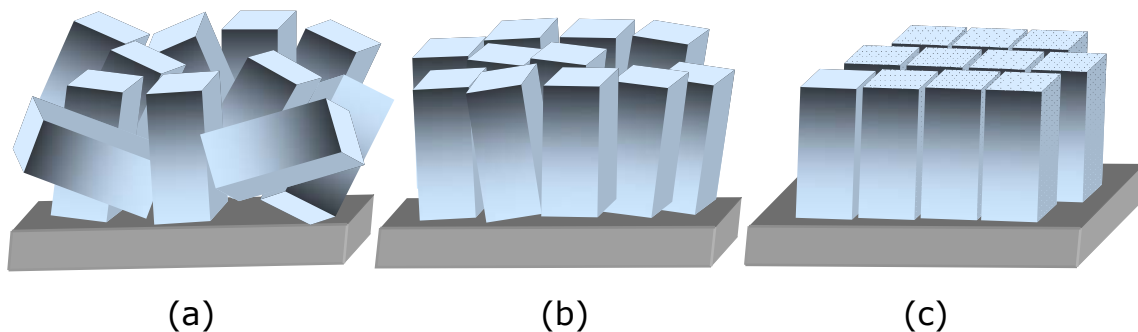


Figure 21. Schematic diagram of crystallites in a) polycrystalline film with weak orientation, b) textured film with preferred orientation and c) epitaxial film with strong orientation [90]

Figure 21 a shows the schematic diagram of randomly oriented crystallites in polycrystalline films, textured films with preferred weak orientation and epitaxial film with strong orientation [90]. A strong orientation has seen to lead to anisotropic properties in thin films [92].

Figure 22 shows a photograph of the Philips X-pert XRD machine available at NREC (Nanomaterials Research and Education Center). The different parts of the system have been labeled to elaborate the equipment more clearly.



Figure 22. Pananalytical X'pert Pro MRD

- XRD Analysis of Sputter As-deposited BST Thin Films

Figure 23 gives a comparative XRD for 3 different BST thin film wafers with conditions described in the previous sections and figure 14.

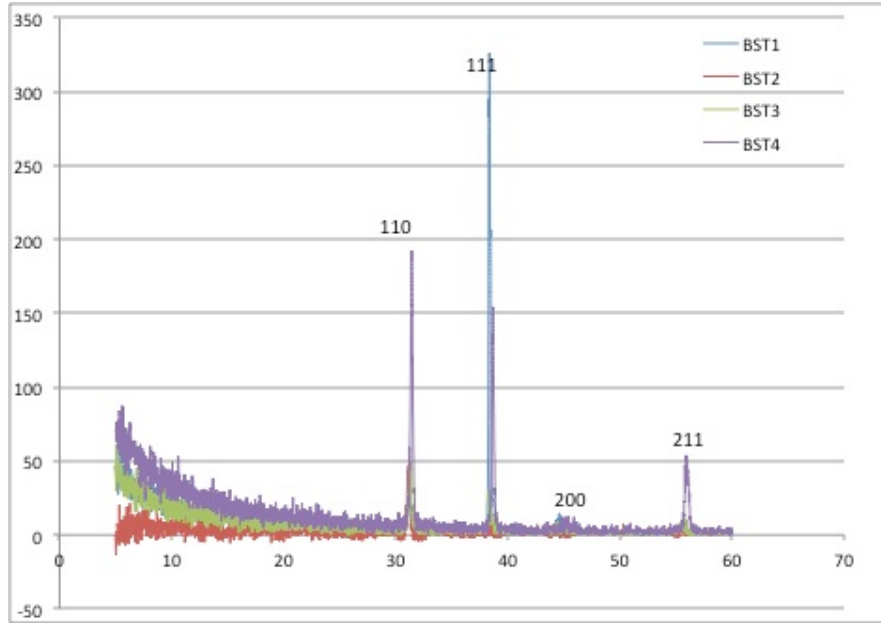


Figure 23. XRD patterns of Sputter deposited BST thin films

- XRD Analysis of Sol-Gel deposited BST Thin Films

Figure 24 shows the XRD pattern of the sol-gel deposited BST thin films. Two XRDs were recorded for films with 1 and 2 spin-coats of BST sol-gel.

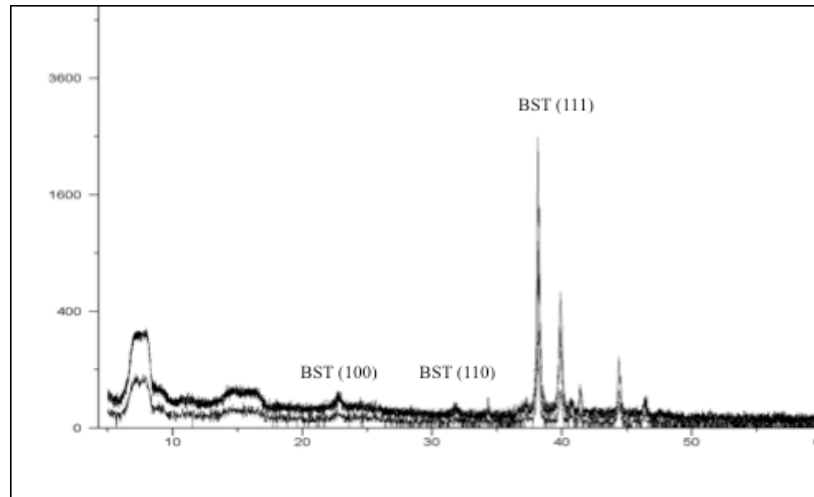


Figure 24. XRD of sol-gel process deposited BST thin films

Figure 23 and 24 display the XRD patterns of different sputtered and sol-gel deposited films. Available literature supports the existence of the (110) and (111) peaks as BST signature peaks [81, 82]. The (110) peak corresponds to the crystalline phase of BST. Thus, in case of RF sputtered films a good crystalline phase was obtained, since the (110) peak looks sharper whereas the (111) peak in these same films are not prominent as that in figure 23. As noted earlier [81] BST sol-gel films tend to shift the (111) peak towards $2\theta=40^\circ$ as the concentration of Barium increases in BST film. The results obtained in our study are in conjunction with previous results. A small bump is seen in Figure 24 where the sol-gel sample is annealed at 700°C . This bump does not continue to develop below 700°C annealing temperature in sol-gel samples. The crystalline peak at (110) in sputtered films is prominent as compared to those in sol-gel films. The (110) peak in sol-gel films does not disappear but is diminished in intensity. As observed in Figure 24 the counts for the peaks are much higher than that for Figure 23.

- Comparative XRD studies of sputtered, sol-gel and stacked films

In order to understand the effect of using different methods studied the XRD patterns of the films deposited using different methods and compared them. Figure 25 shows the XRD comparison between sputtered and sol-gel films after annealing the samples for 12hrs at 900°C .

It can be seen that the peaks look more sharp and pronounced after annealing. This is due to the crystallization of the thin film after exposure to high temperatures.

Figure 26 shows the comparison between sputtered, sol-gel and stacked films. Even though the (113) is less prominent in the sol-gel film, due to the way the sputtered films are oriented, the (113) 'replicates' the orientation in the stacked films too. Figure 27 shows the diminishing (113) peak after annealing for longer time durations. The intensity of this peak becomes less in comparison to the other peaks because of the recrystallization of the films.

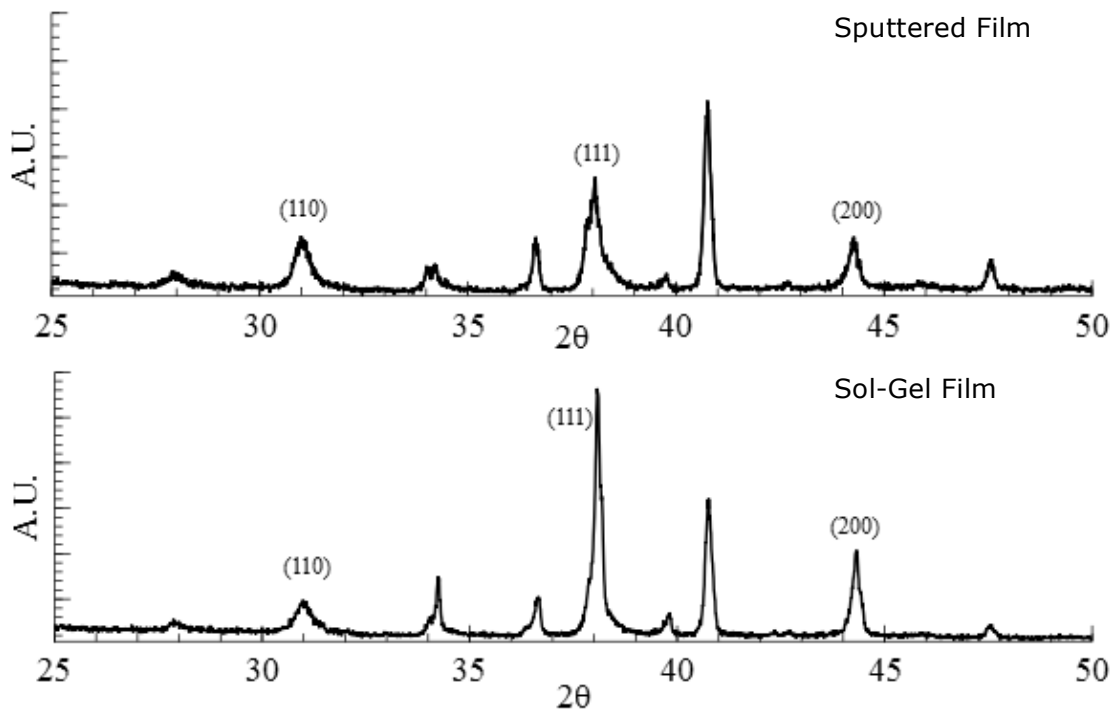


Figure 25. Comparative XRD for sputtered and sol-gel process deposited BST thin films

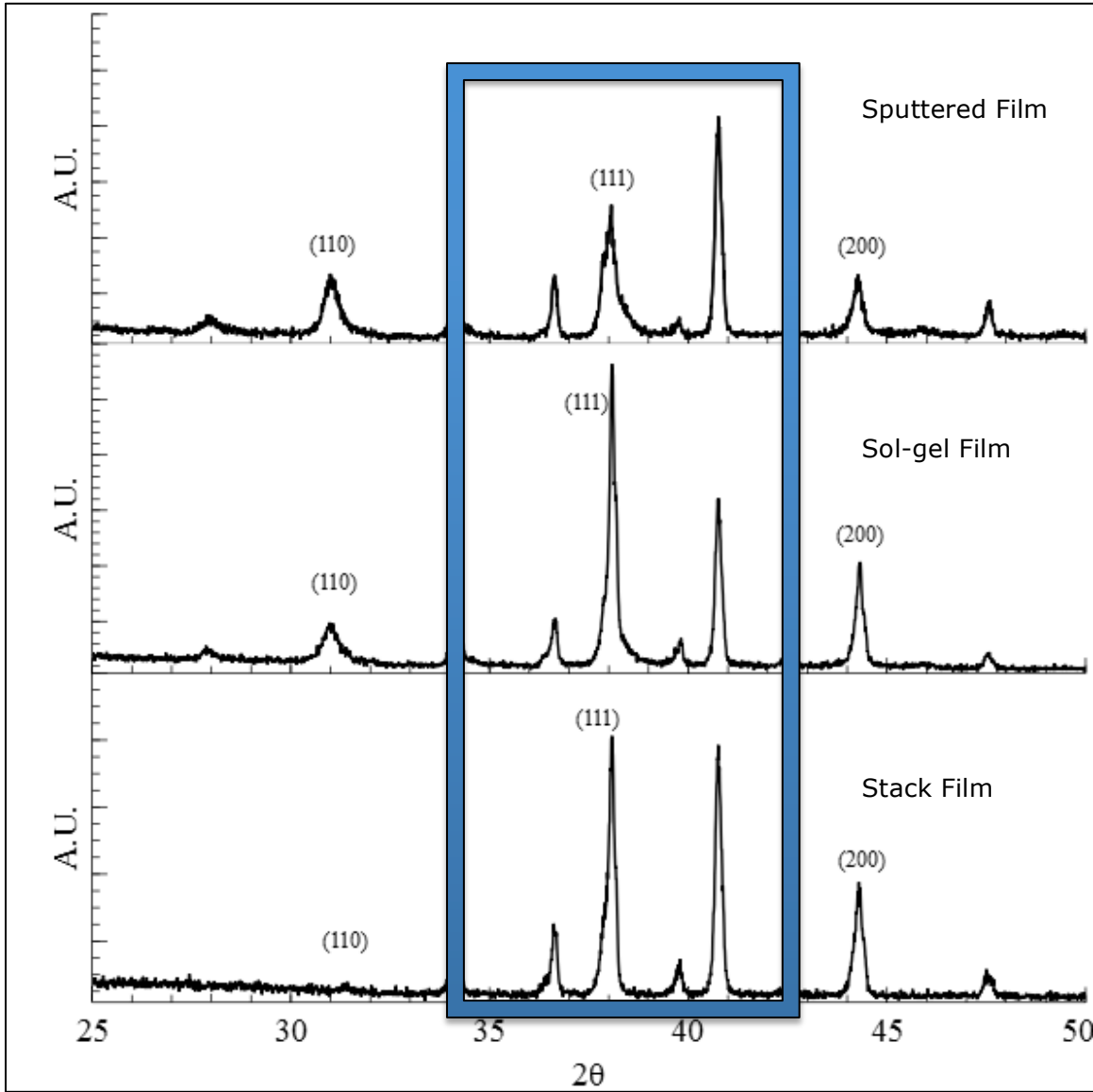


Figure 26. Comparative XRD between sputtered, sol-gel and stacked BST thin films

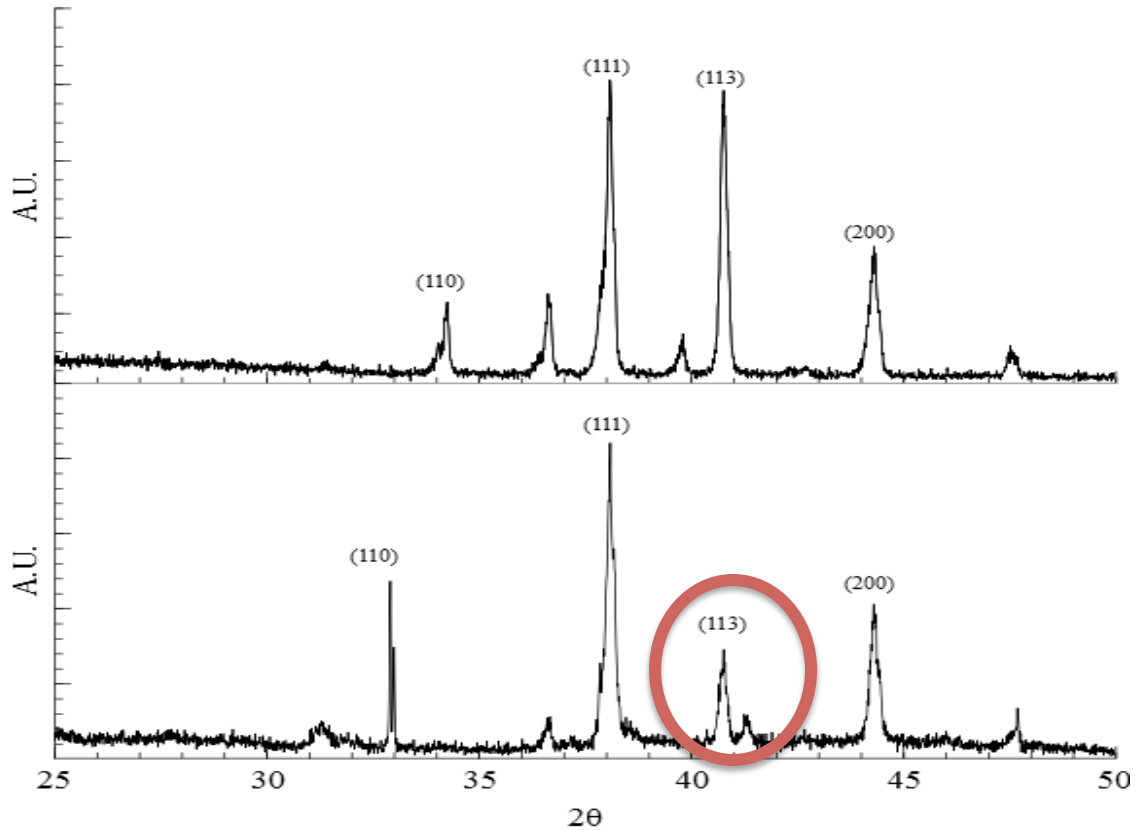


Figure 27. XRD of diminishing XRD peak for stacked BST thin film

Microstructural SEM Studies

Figure 28 (a and b) shows the SEM micrographs of the sputter and sol-gel deposited BST thin films. Figure 28 a) & b) illustrate the SEM micrograph of the sputtered and sol-gel deposited BST thin film, respectively taken at 6000X. The SEM micrograph of sputtered film (figure 28a) shows higher particle size and crystallinity. On the other hand, the sol-gel film (figure 28b) shows a smaller particle size as compared to the sputtered films. This could be attributed to the difference in annealing/sintering conditions after the deposition. It has been reported elsewhere that

microstructure of the films plays a crucial role in the voltage tunability of the device [83]. Sol-gel BST films show more porosity as compared to sputtered films since they have more amount of organic material which burns out during sintering.

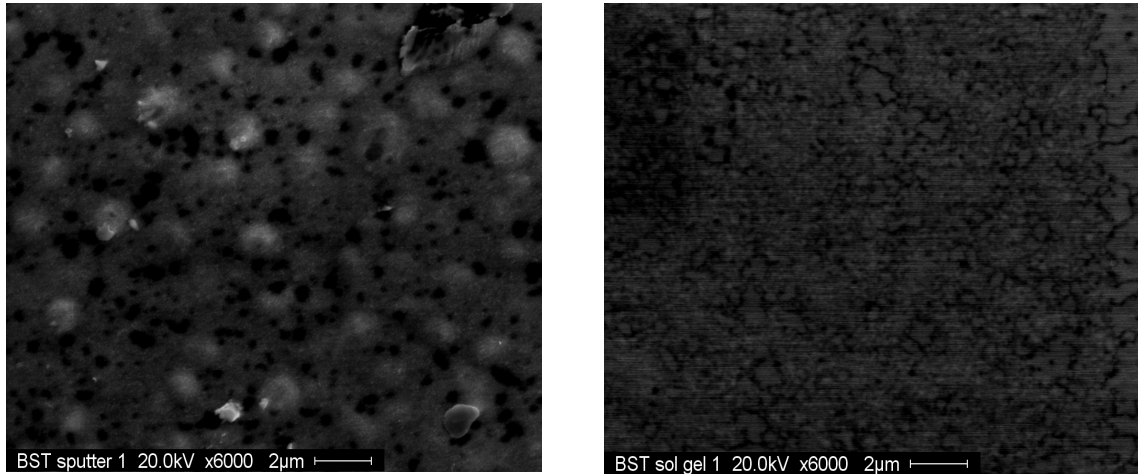


Figure 28. SEM micrograph of a) sputtered and b) sol-gel deposited BST thin film

Cross-Sectional TEM Studies

Transmission electron microscope (TEM) is a powerful tool which is used in the present study to understand the grain boundaries and orientation. A Technai T20 TEM system shown in figure 29 was used for studying the samples. The sample preparation was done using a Quanta 200 3D Dual Beam Focused Ion Beam (FIB) instrument. Figure 30 shows a low magnification cross-section of the sample with BST thin film annealed at 900°C for 12 hrs. A closer look (higher magnification) reveals the different microstructural features of the film.



Figure 29. Technai F20 TEM available in NREC USF

Figure 30 shows the cross section of the BST stack thin film deposited on platinized silicon substrate. Figure 31 shows the TEM cross-section of the BST stack thin film deposited on platinized silicon substrate with higher magnification micrographs showing the crystalline structure on the sputtered and sol-gel film sites, respectively. The structure in figure 30 is a direct representation of how the MIM device looks in cross-section. Figure 31 shows higher magnification of the sputtered and sol-gel layer's crystallinity in the film. It can be seen from the zoomed in insets that the first layer closer to the silicon substrate, being the sputtered deposited BST thin film, which is approximately 250nm comprises of a columnar polycrystalline phase. On the other hand, BST layer above the sputtered deposited layer, which corresponds to the layer deposited using sol-gel technique does not

show a specific growth geometry, suggesting a weak polycrystalline orientation as described in detail in the previous sections. A grain boundary is encountered when the atomic planes look misaligned. Tony et. al [35] has shown in his report the effect of annealing times on these grain boundaries.

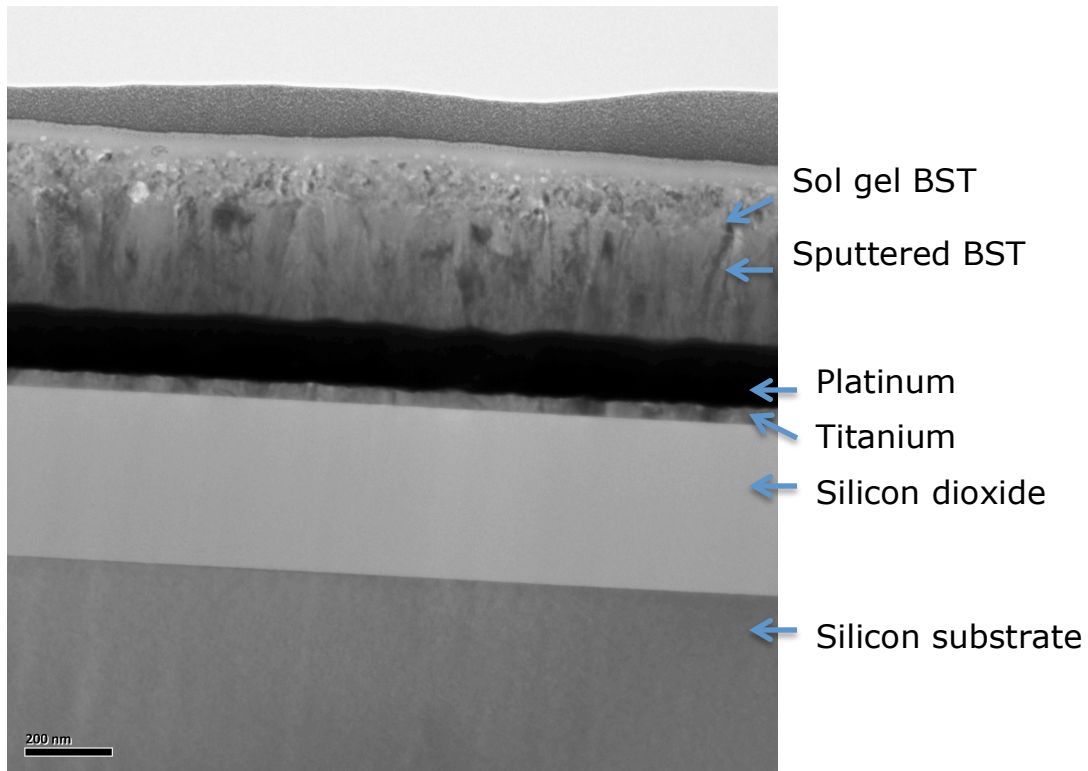


Figure 30. TEM micrograph of BST stack thin film deposited on Pt silicon substrate

TEM images of BST thin film samples give an in-depth information of how deposition takes place and an explanation has been provided in the proceeding sections, for a possible mechanism of leakage current flow through the films with the help of concepts explained in this section.

This apparent difference in the crystallites or grain boundaries facilitates the better electric field behavior in these 'stack' films which will be explained and shown with experiments in the next chapter.

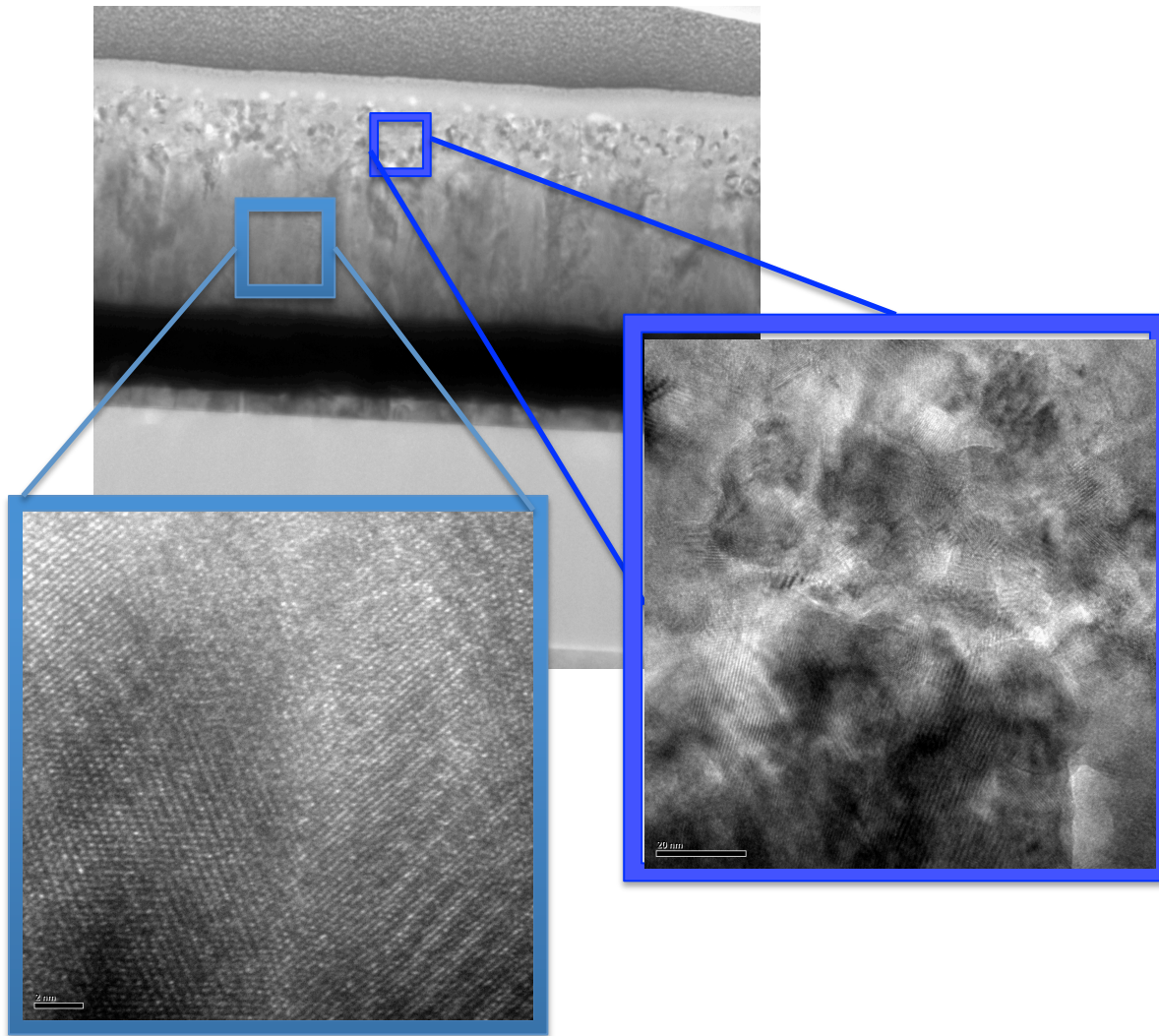


Figure 31. TEM cross-sectional micrograph showing sputtered and sol-gel BST films crystallinity

Surface Roughness Studies Using AFM

Figure 32 (a, b and c) shows the AFM images of BST sputtered, sol-gel and stacked thin films, respectively.

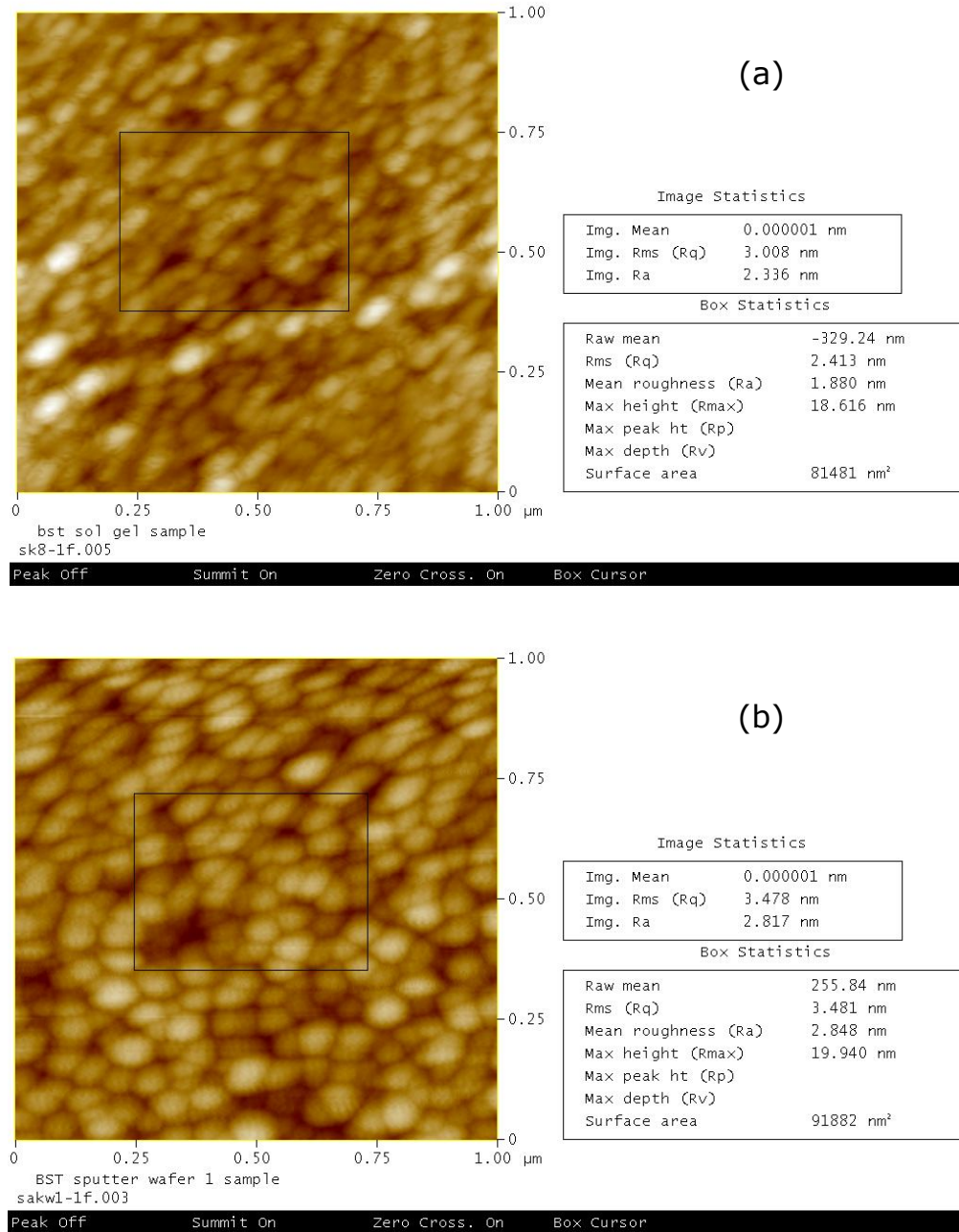


Figure 32. AFM images for BST a) sputtered, b) sol-gel and c) stacked thin film

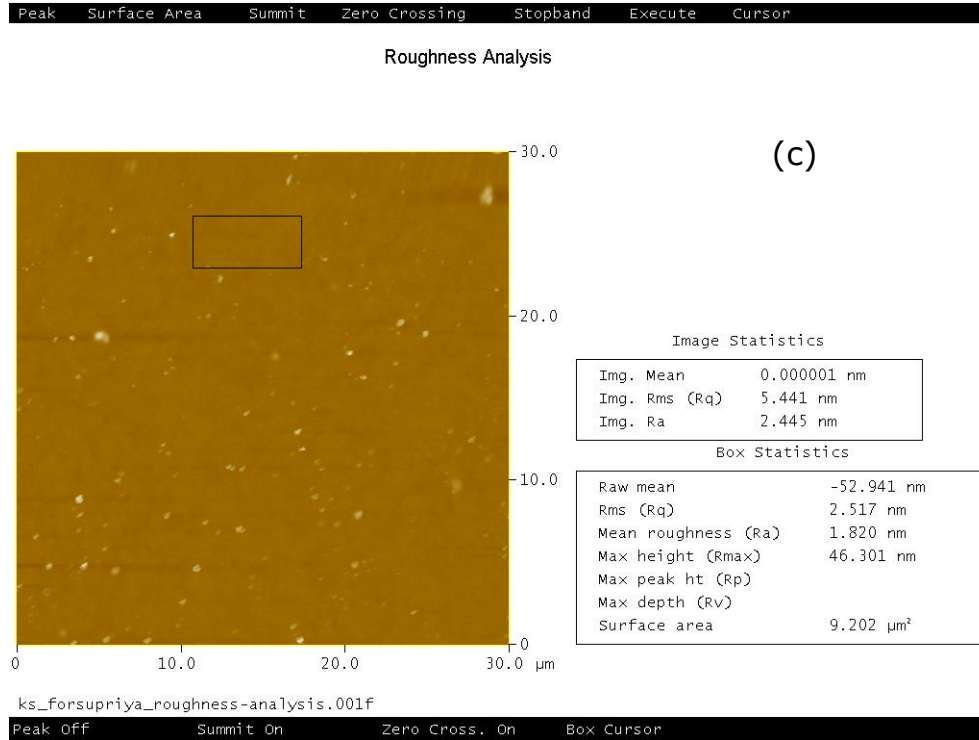


Figure 32. (Continued)

The AFM results for BST sputtered, sol-gel and stacked thin films are shown in figure 32a, 32b and 32c, respectively. The scan area is $1\text{sq.}\mu\text{m}$ for the sputtered and sol-gel thin films and $30\text{sq.}\mu\text{m}$ for the stacked BST thin film. The surface roughness (mean roughness Ra) for the sputtered and sol-gel thin films is in the range of 2-3nm. Even though sputtered films have a smoother coverage over a larger area, there is a tradeoff between thickness uniformity and surface smoothness. Sol-gel films on the other hand can be deposited on smaller areas with similar surface smoothness. At the same time, sol-gel films have an advantage of being processed in a shorter time

[93]. The surface roughness for the stacked film is also in the same range ($\sim 2-3\text{nm}$).

Conclusions

There is a clear distinction between the annealed and non-annealed film structure as evident from the XRD studies. The annealed BST thin films become more crystalline and show a preferred orientation. The TEM images are conclusive of the orientation difference between the sputtered and sol-gel deposited films. The sputtered films clearly show a columnar structure whereas, the sol-gel thin films are randomly oriented. The proceeding chapter gives a relationship between the effect of the crystal structure and the electrical properties of these BST thin films. The surface roughness of the BST thin films deposited by sputtering and sol-gel is in the range of $\sim 2-3\text{nm}$, at the same time, the surface roughness value for the stacked BST thin film is also in the $\sim 2-3\text{nm}$ range, thus suggesting a matching of the roughness parameter which has been a major concern for microwave applications [33].

Chapter 4: Device Fabrication and Electrical Properties of BST Thin Films

Introduction

A range of electrical characterization methods were applied to the BST films studied in this work to assess their performance. DC electrical characterization was carried out to assess the leakage behavior of the BST thin films while AC studies were carried out to determine the tunability of the BST thin films. In general, microwave studies are carried out to understand the interaction between the thin film material and corresponding substrate. Microwaves tend to partially penetrate a metal and flow in a narrow band near the outside surface. The current density falls off exponentially from the surface of the conductor to the center. This signal amplitude falls off to 36.8% of its surface amplitude at a certain depth, called "skin depth". It is common knowledge that microwaves flow freely through dielectric materials inducing net polarization [46].

Device Fabrication Process

MIM Capacitor Fabrication

It is common practice to use either parallel plate or planar device configuration to test BST thin film varactors [94-98]. Parallel plate structures

have an advantage of higher surface area interaction, hence show higher tunability. Planar structures, on the other hand, are easier to fabricate. For the current investigation, we have used metal – insulator – metal structures (MIM) to measure DC electrical characteristics of BST thin films and interdigitated capacitor planar structures to understand their AC high frequency characteristics. Corona-Kelvin Metrology (C-KM) measurements were done on relatively simple device structures. Due to their ease of fabrication, it was a preferred method to study the leakage behavior in these films and then use the same deposition conditions to deposit thin films in MIM or IDC configuration and test their electrical properties.

Parallel plate or MIM structures are more desirable choice for device geometry due to their established higher tunability. A BST film is sandwiched between 2 metal electrodes. The down-side of using MIM configuration is the device complexity due to the bottom electrode. Usually, the metal used as bottom electrode cannot withstand the temperatures the films need to be exposed to annealing. Metals such as gold, aluminum, platinum and nickel tend to react with silicon and form silicides. There have been studies to understand and correct this phenomenon before [99]. Platinum tends to withstand high temperatures but can form hillocks and hence, a careful understanding of the temperature-bottom electrode-substrate interaction was necessary.

The planar structure fabricated for RF tunability measurements had a drawback of field confinement. The external applied electric field does not stay within the film. The capacitance of interdigitated patterns can be manipulated by changing the gap between the electrodes or the length of the electrodes. Basically, the electric field confinement governs the capacitance of the device. As the gap width is reduced, the capacitance is seen to increase. Hence, interdigitated patterns are an attractive solution for designing RF tunable device test structures.

Patterning BST Thin Films

1. Approach 1: This device configuration consisted of depositing BST thin films on silicon wafers. Details of deposition parameters and conditions were discussed in chapter 3. Once these 6" wafers were deposited with BST thin film, they were diced at NREC using the Microteck dicing saw. Samples of 15mm x 15mm were diced. These samples were primarily made for different annealing temperature recipes and CKM electrical measurements. After dicing the samples were cleaned using DI water, acetone, methanol and IPA. The cleaned samples were then annealed at different annealing temperatures and ambients. Table 5 shows the different annealing conditions used for the experiments.

Table 5. Experimental matrix for annealing conditions for BST thin film samples

Annealing temperature (°C)	Annealing time (hrs)	Annealing atmosphere
400	6	Air
600	6	Air
800	6	Air
900	6	Air
400	12	Air
600	12	Air
800	12	Air
900	12	Air
400	6	Oxygen
600	6	Oxygen
800	6	Oxygen
900	6	Oxygen
400	12	Oxygen
600	12	Oxygen
800	12	Oxygen
900	12	Oxygen

2. Approach 2: Figure 33 shows the fabrication steps of the BST MIM capacitor structure. The Pt and Ti depositions were carried in the CRC sputtering tool. The thickness measurement of each of the layers was

done using Dektek profilometer. Aluminum was thermally evaporated as top electrode.

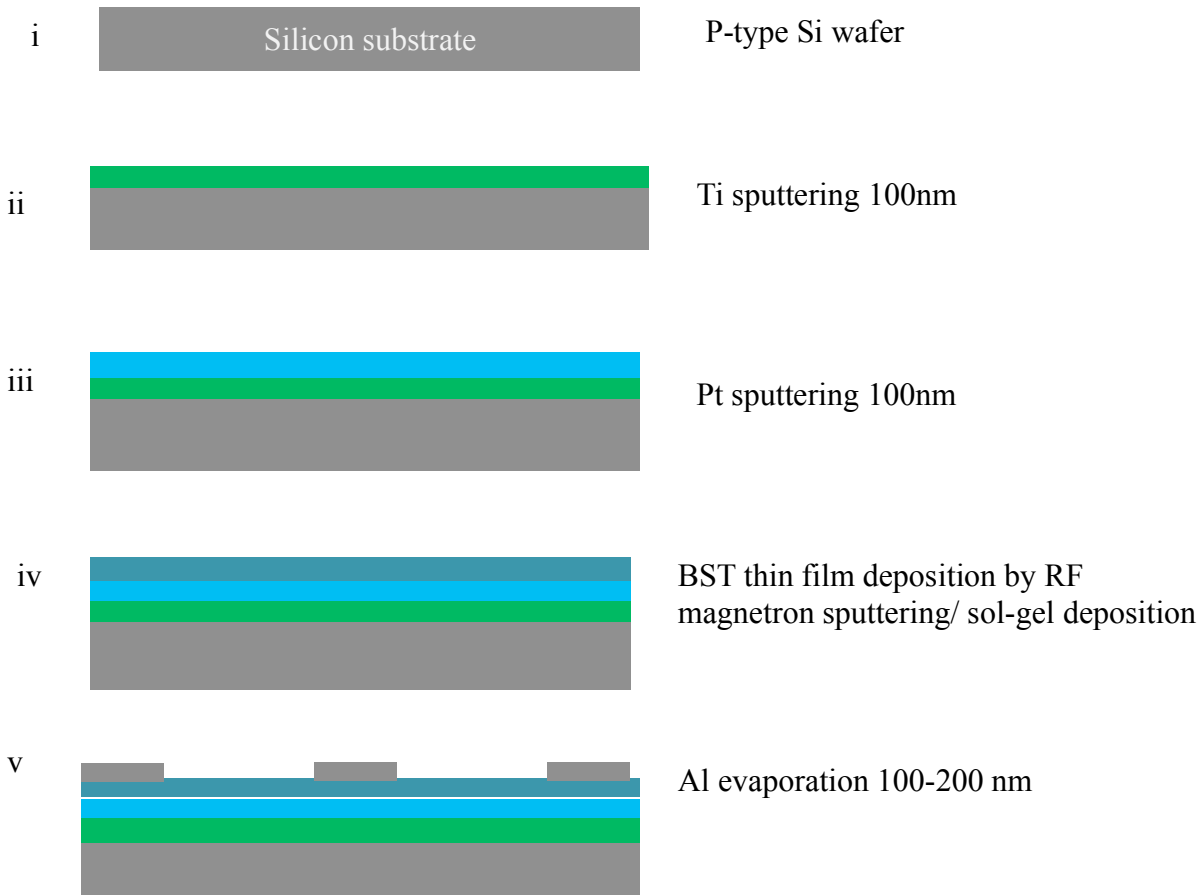


Figure 33. BST thin film MIM structure fabrication process

3. Approach 3: Interdigitated patterns were fabricated on alumina, sapphire and MgO ceramic substrates with varying gaps and widths to study the 'tunability' of these films. A detailed description of the samples and their fabrication procedure [21] is given in Appendix D. To begin with, BST thin films of thickness of around 250nm were deposited on 16 different types of substrates (alumina, silicon,

sapphire and MgO) using the deposition recipe given in table 3. After deposition, the films were annealed at 900°C for 12 hours in either air or oxygen ambient at a 4 liter/min flow rate. Shipley 1813, a positive photoresist, was used as a mask layer to prevent sections of BST layer from being etched away. The photoresist patterning was carried out on the quintel mask aligner at NREC. After patterning the photoresist, the BST thin films were subjected to BOE (buffered oxide etch) with 6:1 ratio, which was inefficient in cleaning some surfaces of the film. Annealing the BST thin films made them harder to etch away in standard BOE solutions and hence, time and concentrations were varied to ensure proper etching of the films. This problem is not observed for films, which are not annealed. Some DRIE 'cleaning' recipes were also used for patterning the BST films properly. To use DRIE, a thicker photoresist Shipley 1827 was used to protect the pattern. Once the patterning was done, the photoresist was removed following regular photoresist stripping process or using oxygen plasma.

The top electrodes for the interdigitated pattern were fabricated by using a negative photoresist mask Futurexx 3000PY and then, thermally evaporating a layer of Cr (chromium) for adhesion followed by Au (gold) as top electrode. The total metal electrode thickness was obtained to be 800nm. Denton DV-502A thermal evaporator with a capability of depositing

2 metals was used for this process. A lift-off was performed using Futurex RR41 resist remover heated to 100°C. Figure 34 (a, b and c) shows the final BST thin film interdigitated patterns used for Thru, Reflect, Line (TRL) measurement. Figures 34a, 34b and 34c show the 3, 5 and 7 finger interdigitated patterns on the alumina, respectively. The fabricated BST thin film IDCs were electrically tested using DC as well as AC measurement techniques. Capacitance-voltage measurements were recorded on the samples using HP 4284A LCR meter by sweeping the voltage from negative 40V to positive 40V at 1MHz frequency.

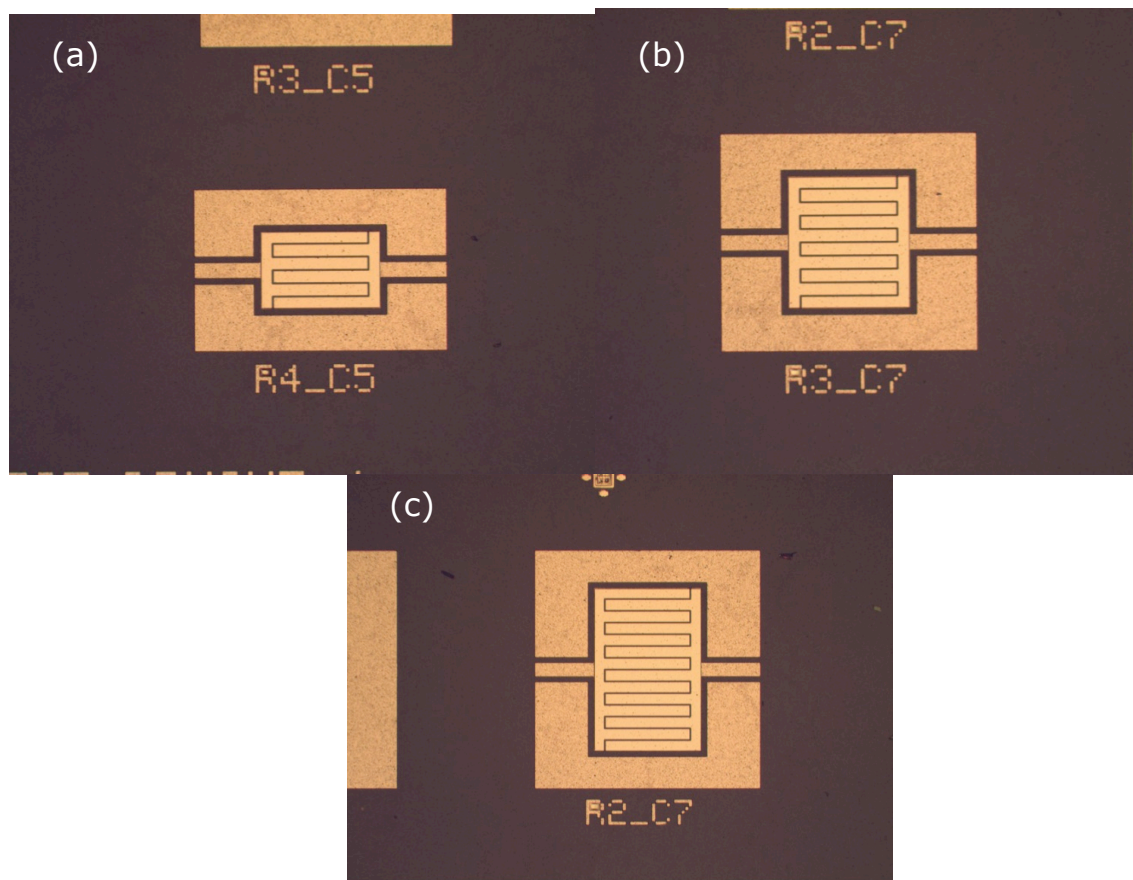


Figure 34. Interdigitated BST thin film pattern on Alumina substrate with a) 3 fingers, b) 5 fingers and c) 7 fingers

Electrical Characterization of BST Thin Films

It is common for BST to have very low band offsets and high leakage current as other high-k dielectric materials [100]. In parallel to high-k capacitance a conductance is introduced due to small band offsets causing substrate gate injection or band injection. Three types of electrical measurements were carried out on the samples, DC, AC (high frequency) and Corona-Kelvin non-contact metrology DC measurements.

Small Signal AC Measurements at Set DC Bias

Figure 35 shows the electrical response at high frequency recorded at fixed DC bias of a 7-finger IDC device measured using the HP4284A LCR meter. The graph shows 3 responses recorded at 100KHz, 500KHz and 1MHz. A tunability of 20% was observed in these samples.

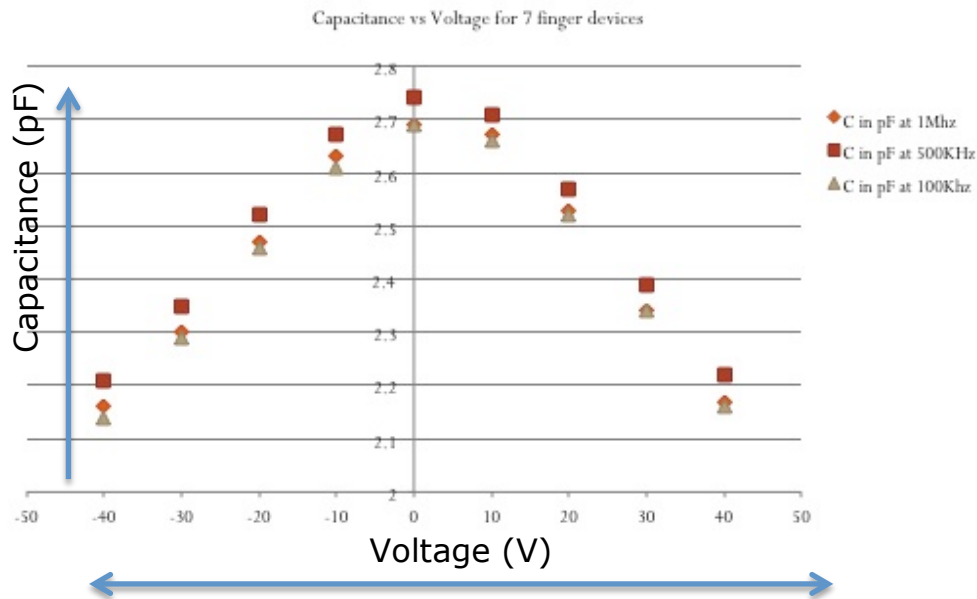


Figure 35. CV response of BST thin film sample deposited on alumina substrate for a 7 finger device using HP 4284

Corona-Kelvin Metrology

Application of bias is required across the oxide/semiconductor barrier to measure capacitance-voltage characteristics of a dielectric. This is conventionally achieved by depositing a conducting metal electrode such as aluminum (Al), gold (Au), platinum (Pt) or polycrystalline silicon. An electrical probe contacting the dielectric/semiconductor structure biases the structure relative to the counter electrode, typically grounded.

Methods, which require device fabrication for contacts are too complex, time consuming and limit the possibility of continued processing after the characteristics of the dielectric/ oxide have been established. So an extensive need for discarding or building test wafers/ samples is required. Also, the time spent in fabricating these devices is unnecessary in a research and development environment where a quick and easy solution is required for optimization of processes. Figure 36 gives a comparison of processes that can be used to measure the capacitance – voltage characteristics of an oxide surface.

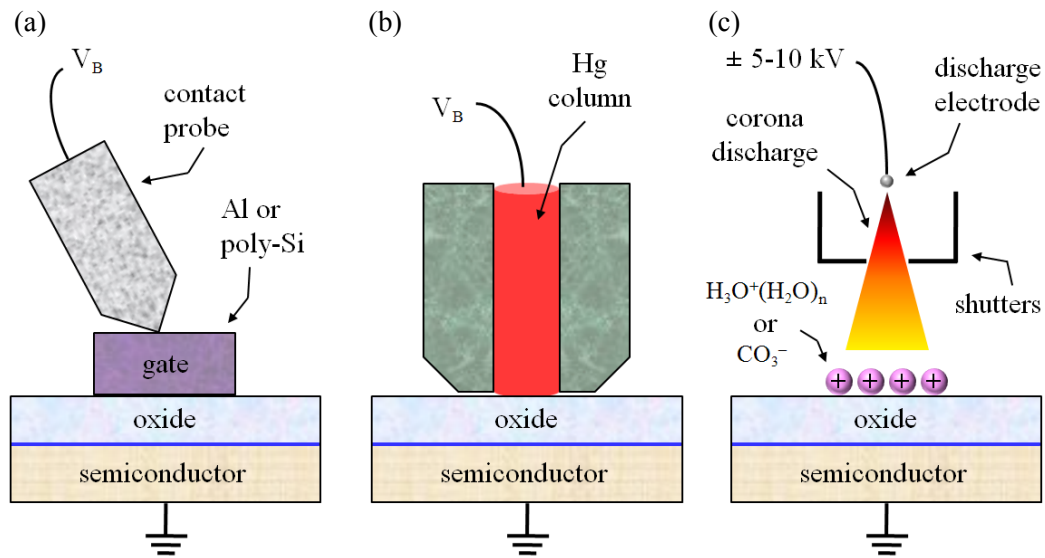


Figure 36. Bias generating techniques across an oxide/semiconductor structure, a) MOS contact, b) Hg-probe and c) corona-ion deposition [adapted from ref 123]

In Hg-probe, the mercury provides a temporary electrical contact with an oxide surface. Hence, Hg-probe can provide C-V measurements without the need of a test structure. But, an Hg-probe leaves residual mercury metal on the surface of the device under test, after measurement. Thus, making the surface dirty and requiring a cleaning step if the oxide needs to be processed further.

Corona-Kelvin metrology (C-KM) works on the principle of depositing corona ions on a surface and monitoring the potential of the structure with a non-contacting probe. This is an in-line metrology technique and hence, is non-invasive, fast and can be used to obtain oxide electrical characteristics at selected points in a sequence of processes [105-110]. The C-KM technique charges air to generate CO_3^- or $\text{H}_3\text{O}^+(\text{H}_2\text{O})_n$ ions and deposits them on the sample surface. The main advantage of this technique is that

these ions are non-damaging and can be removed from the sample surface by simple DI water rinsing. Figure 36c shows an illustration of how the technique works. The charges accomplish the charging of the oxide/semiconductor surface just like in MOS C-V measurements. Due to its innate nature of non-contact probing by measuring the deposited charge and the resultant voltage difference, this method is useful in extracting crucial electrical measurements. It produces charge and voltage information which is the figure of merit for semiconductor, dielectric and oxide measurements. Thus, C-KM provides a non-invasive, in-line electrical monitoring tool for dielectrics, semiconductors and oxides. Figure 37 (a, b and c) shows the schematic of a typical C-KM metrology tool and its working along with the actual probe used in our lab to take these measurements.

Corona-Kelvin Metrology has been employed in the present investigation to measure the contact potential difference voltage of sputter deposited BST films. Traditionally, determination of electrical properties such as permittivity, loss tangent and tunability required deposition of ring resonators or similar transmission line structures onto the films followed by microwave characterization and use of one or several approaches for parameter extraction. C-KM does not require electrode deposition to determine electrical parameters. Consistent with past IV-CV data the C-KM data showed high conductivity at moderate, (few volts/BST thickness), field values.

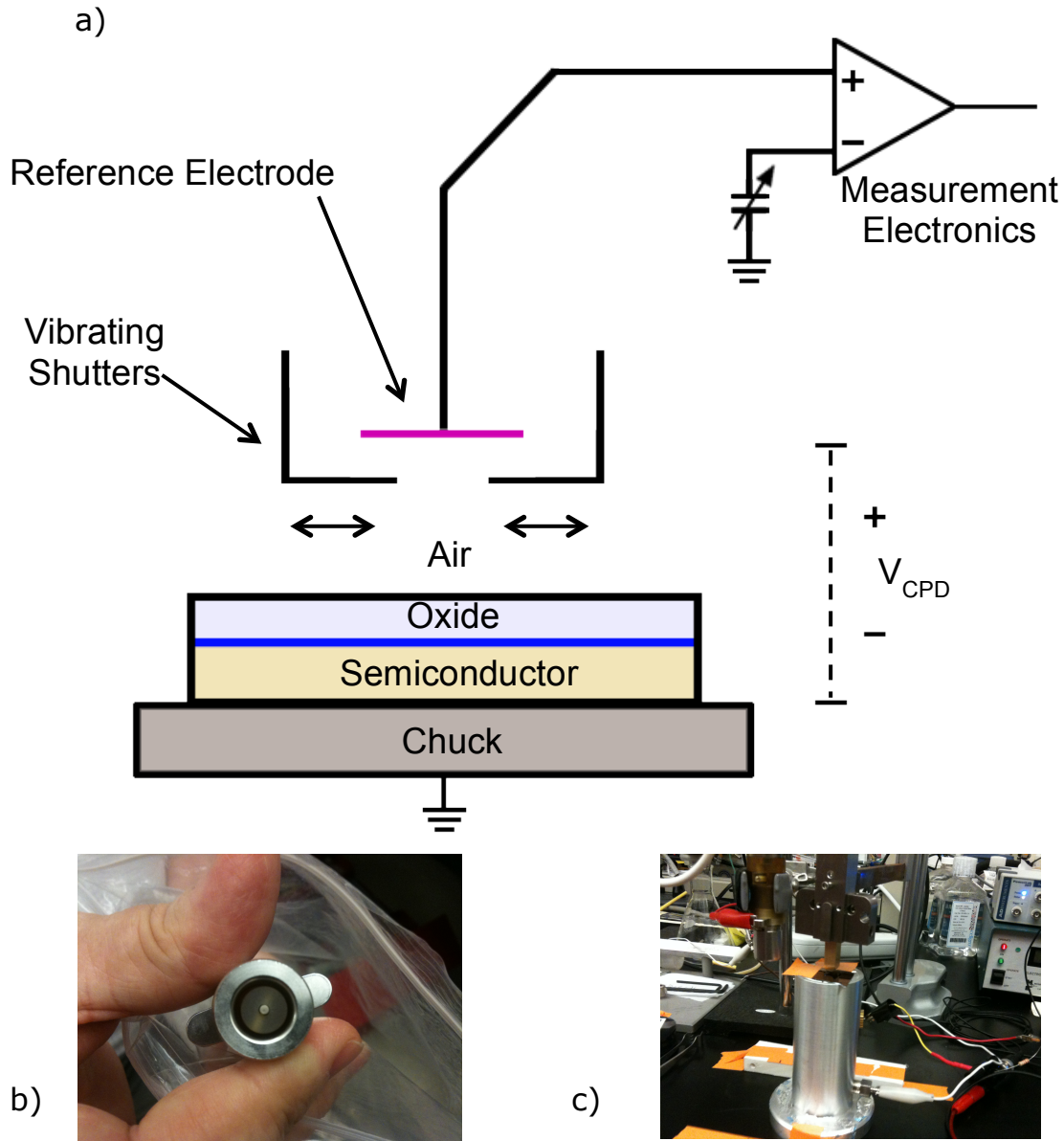
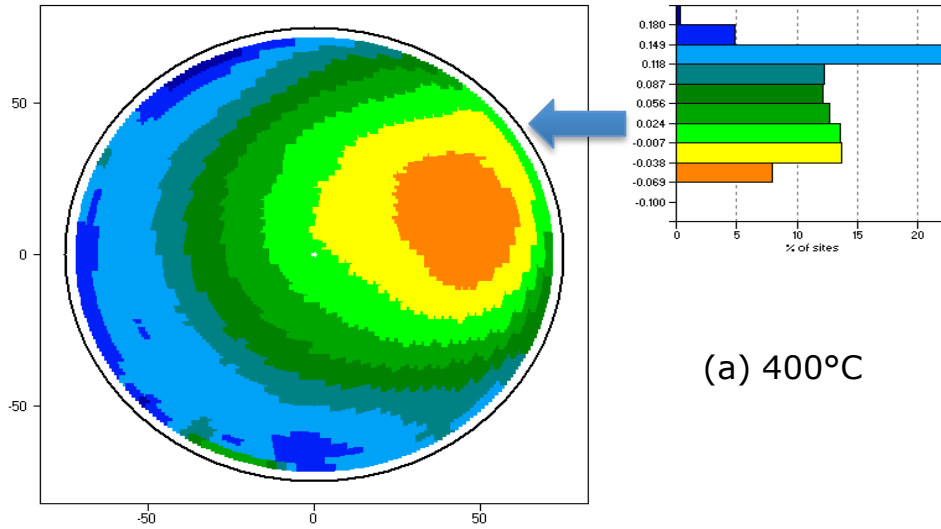


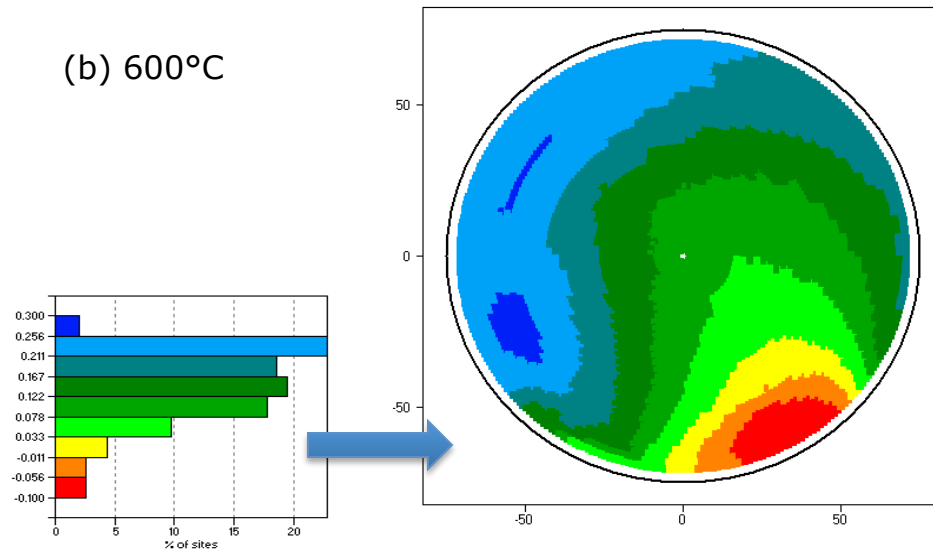
Figure 37. a) Illustration of C-KM set-up, b) Corona ion source and c) Kelvin probe potential measurement set-up [123]

C-KM determined as-deposited parameters such as charge in the thin films. This is demonstrated in Figure 38a and b where the range in contact potential voltage is a measure of the variation of charge in the as-grown

films, assuming that the thickness variation of the films are minimal. Note that charge persists even at moderate deposition temperature.



(a) 400°C



(b) 600°C

Figure 38. Vcpd maps of as deposited BST thin film wafers deposited at a) 400°C and b) 600°C

Regardless of sputtered film measured (independent of annealing and deposition conditions) very small potential drops were created. $V_{CPD} = \phi_{MS} + V_{OX} + V_{SB}$ for as-deposited films, where, V_{CPD} is the contact potential difference (in volts), ϕ_{MS} is the work function, V_{OX} is the oxide potential difference and V_{SB} is the surface barrier potential difference in the semiconductor. Portions of the n-type silicon wafer are in depletion due to negative charges at the interface. The C-KM measurements also yield the effective oxide thickness (EOT). EOT is the ratio of $\epsilon_0 \epsilon_r$ (where, ϵ_0 is the permittivity of vacuum and ϵ_r is the relative permittivity of the medium) for SiO_2 to the measured capacitance of the film equal to $\Delta Q/\Delta V$. The permittivity of the films was estimated using the physical thickness and EOT. EOT for the two films was 70Å and 66Å, from which ϵ_r (permittivity of BST thin films) was found to be 133 and 141 for an average film thickness of 240nm.

Figure 41 display the voltage vs time graphs of sol-gel deposited BST thin films, obtained using the C-KM tool. A fixed charge was deposited every 2 seconds on the as-deposited BST films and studied over a fixed time for leakage. For every finite charge added the voltage should increase by a constant value if the film capacitance is constant and leakage is not present. The voltage was swept from negative to positive value and then from positive to negative for each sample to check the maximum voltage it can withstand without leakage. Figure 39a and b displays the graph for sol-gel

deposited sample annealed at 800°C peak temperature for 5hrs. It is seen that the voltage starts to saturate around 0.15V negative and also shows leakage, indicated by slope in the characteristic following charge deposition. Also, in the positive direction voltage is seen to saturate at around 2.5V. Thus, it can be concluded that the film prepared will leak outside the operating voltage range of 2.5 to -0.15V. The bending of the response in graphs 41a and b is due to leakage or trapping of charges.

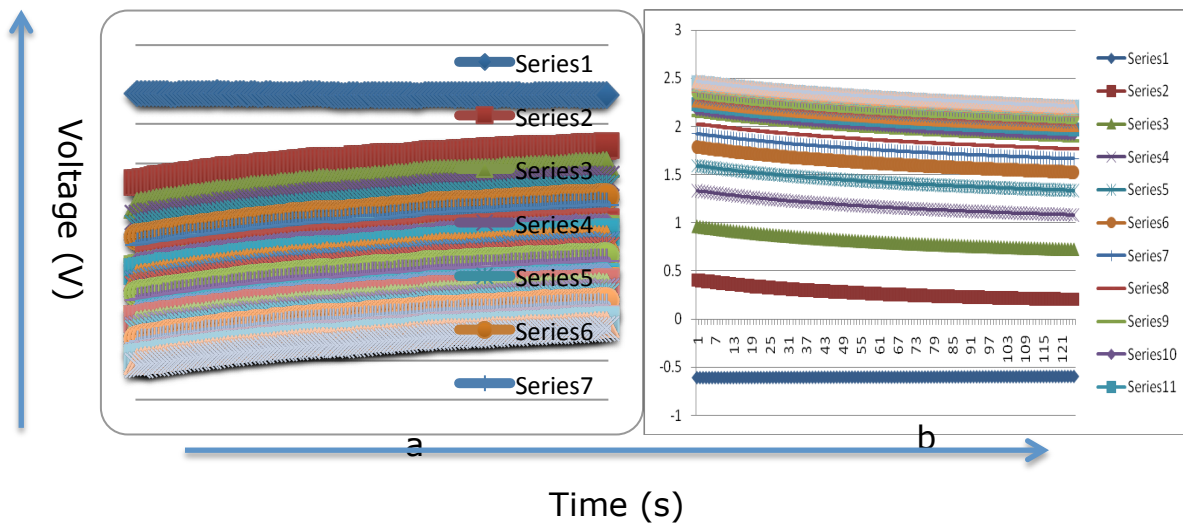


Figure 39. Vcpd transient decays with consecutive repetitions of corona deposition spaced at 2s intervals obtained on sol-gel deposited BST film annealed at 800 deg C voltage swept from a) positive to negative and b) negative to positive

A similar response was observed for films deposited using rf magnetron sputtering. Figure 40 displays the voltage vs. time graph of stack-BST deposited thin films obtained using the Corona Kelvin metrology tool. The films were deposited on plain silicon substrates. A standard RF magnetron sputtering deposition process was followed to deposit

Ba_{0.6}Sr_{0.4}TiO₃ on the substrate. Sputter deposition was followed by sol-gel spin coating with the procedure described earlier in this report. As seen from the graph, there is a significant amount of improvement in the voltage that can be handled by these films. The films can withstand up to 18V positive and more than 25V negative. This marked improvement in voltage capacity can be attributed to the higher thickness and dense-crystalline morphology of the BST films.

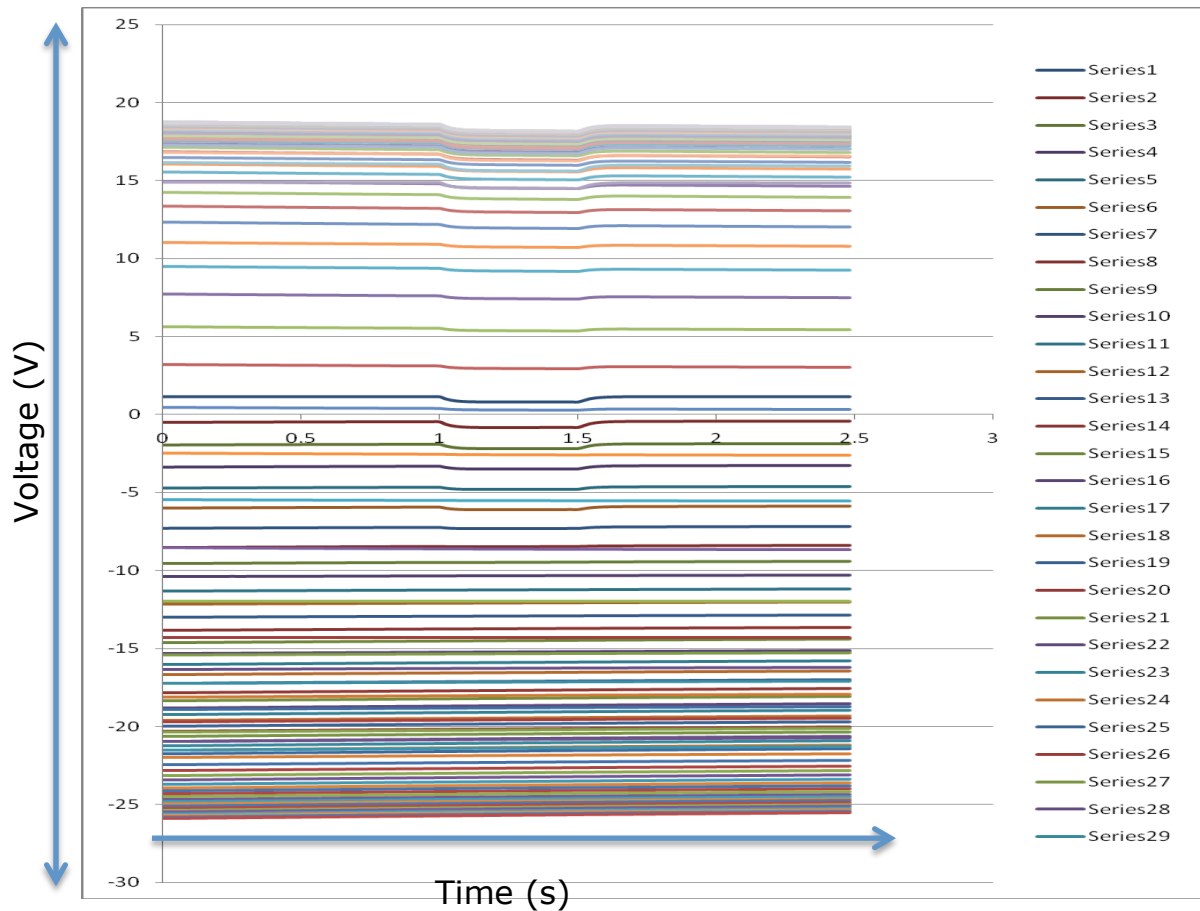


Figure 40. Vcpd transient decays with consecutive repetitions of corona deposition spaced at 2s intervals, obtained on stack BST sample annealed at 600 deg, voltage swept from 0 to 18V and from 0 to negative 25V

Table 6 shows the different voltages applied (both positive and negative) and the voltages sustained by different BST thin film samples deposited on silicon as well as platinized silicon samples. It is clear from the data given in the table that the 'stacked' BST thin film samples were able to withhold the most potential in both positive and negative directions.

Table 6. Comparative table of voltages sustained by different types of samples in positive and negative direction, data recorded using 6KV power supply.

Sample Type	Max Voltage applied (+ve) In Volts	Max Voltage sustained (+ve) In Volts	Min Voltage Applied (-ve) In Volts	Min Voltage sustained (-ve) In Volts
Sputtered BST Films on Si substrate	100	33	-86	-75
Sputtered BST films on Platinized Si substrate	80	35	-78	-13
Sol gel BST films on Si substrate	100	59	-89	-34
Sol gel BST films on Platinized Si substrate	80	38	-80	-41
Stack Films on Si substrate	103	58	-86	-50
Stack Films on platinized Si Substrate	100	58	-90	-50

The data was collected using a Kelvin probe with a power supply of 6KV. The prepared samples with the described deposition parameters, which meet the voltage-sustaining criterion, can be then passed on for further processing. So, a few samples deposited using similar conditions were sent for further studies to SDI lab facilities. Figure 41 shows the transient response of a BST RF magnetron deposited thin film sample for a positive sweep from 0 to 30V. Graph 41a displays the voltage-charge (V-Q) plot for BST RF sputter deposited thin film sample of thickness 300nm.

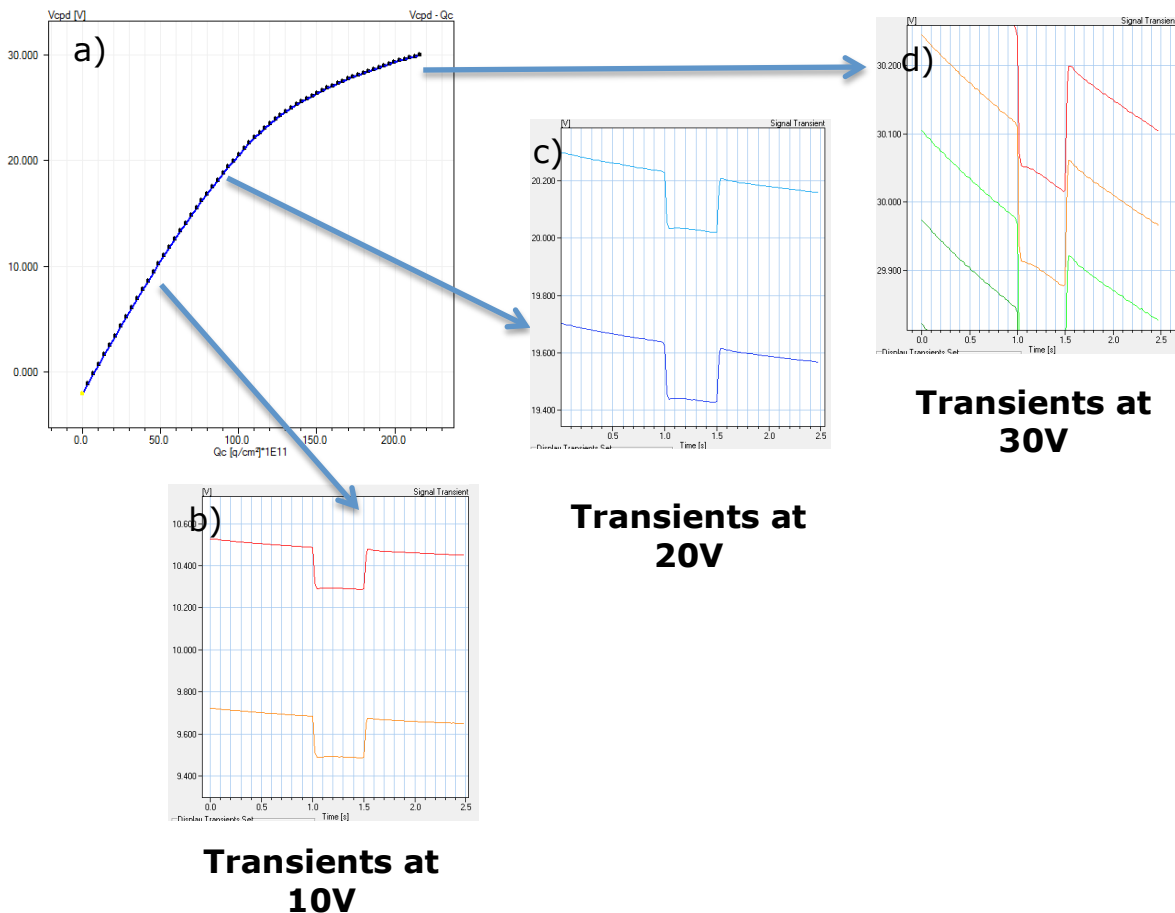


Figure 41. a) Transient C-KM response of a BST thin film sample C2, response over 2s time interval at b) 10V, c) 20V and d) 30V.

The slope of the response is seen to change over a range of 0 to 30V (positive sweep). This phenomenon can be attributed to the change in capacitance ($C=Q/V$) over change in voltage, which is expected. The transient responses measured over ~ 2.5 seconds with a few chargings, shown as stacked plots, at nominal voltage values of 10V, 20V and 30V, respectively. There is a slight drop in the overall voltage over a period of ~ 2.5 s in each of the transient responses. This could be due to the leakage charge from the BST layer to the silicon and hence, ground. The 'dip' in the transient responses is because of the 'light on' duration. This 'dip' is equal to the voltage drop across the BST dielectric thin film layer since the 'light off' voltage drop corresponds to the combined voltage drop across the silicon substrate and the dielectric thin film. This is given by,

$$V_{CPD} = V_{SB} + V_{OX} \quad (4.1)$$

where, V_{CPD} is the contact potential difference, V_{SB} is the surface barrier voltage and V_{OX} is the voltage across the oxide. When the light is turned on, V_{SB} is zero hence $V_{CPD} = V_{OX}$. This comes from the difference in V_{cpd} dark – V_{cpd} light that eliminates the ϕ_{ms} term and gives unique V_{ox} at a given charge value. The total V_{ox}/Q curve provides capacitance. Therefore for the above sample, $V_{CPD} = 30 - 0.2V = 29.8V = V_{OX}$. For each of the transient responses, this voltage drop is approximately 0.2V. Thus, we can conclude that the voltage drop due to the dielectric is the total voltage drop minus 0.2V at any given point (the surface barrier is constant over this range).

It can be also seen from the different transient responses (a, b and c) that the surface barrier differs from each other, that is, the V_{SB} at 30V is approximately 0.35V whereas, at 10V it is 0.2V. Figure 42 shows the negative sweep of the same sample from 10V to -10V. It is observed that the surface barrier remains the same ($\sim 0.2V$), suggesting no change in the trapped charges.

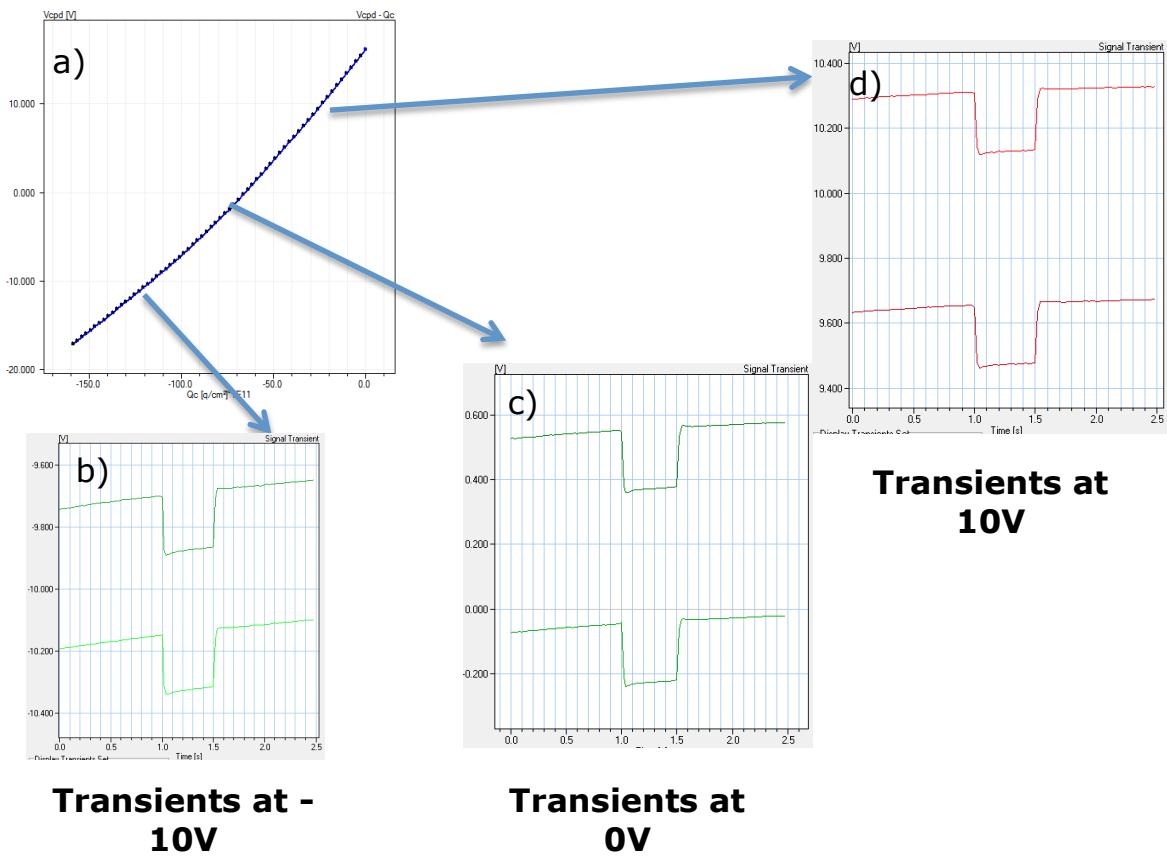


Figure 42. a) Transient C-KM response of BST thin film sample C2, response over 2s time interval at b) -10V, c) 0V and d) 10V swept from positive to negative

Figure 43 recorded on a different sample, C3, suggests a change in the surface barrier voltage when swept from 0 to 30V followed by 20V to -30V.

Even though the positive sweep surface barrier potential difference was recorded 0.35V. This voltage drop goes to less than 20mV (almost 0V) when the same sample is swept to -30V. This phenomenon is proof of the existence of trapped charges. Note again that the surface barrier is increased going positive but once there in the negative it does not change.

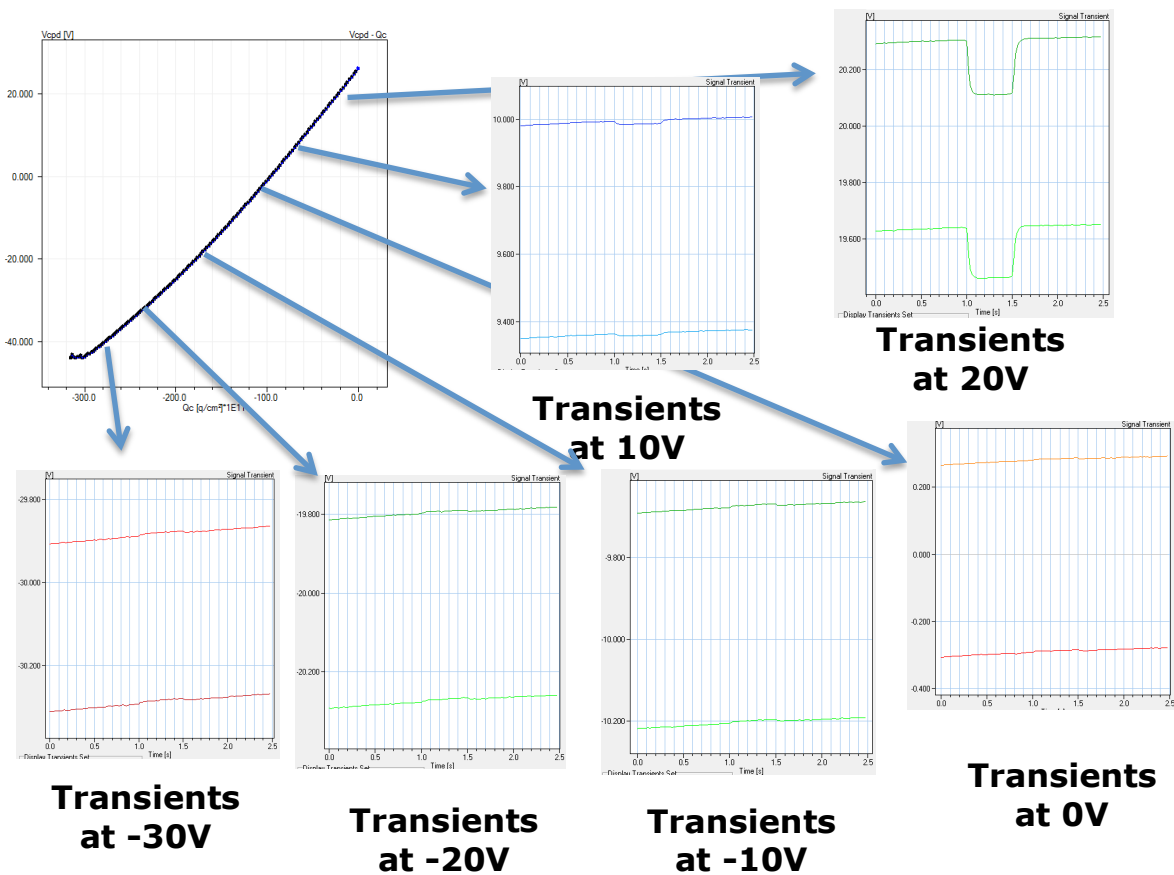


Figure 43. Transient C-KM reponse of BST thin film sample C3, response over 2s time interval at various voltages showing evidence of trapped charges

We can conclude from the above C-KM responses that, going to positive voltage the sample goes into depletion (p-type substrate), the surface barrier increases and goes to maximum and saturates. Whereas,

when negative charges are applied to the same sample, the charges are trapped, and hence the surface barrier goes to 0V showing flatband voltage. $V(\text{flatband})$ is the value of V_{cpd} where $V_{\text{light}}=V_{\text{dark}}$ that happens at a unique value of Q applied. In this sample, positive charging pulled electrons into traps near the semiconductor surface and when negative charge was applied the traps did not release, essentially pinning the surface barrier at a near constant value.

Some important findings of C-KM measurements can be summarized as follows:

1. Certain regions on the Contact Potential Difference (CPD) maps have areas which are more negative with respect to substrate (n-type substrate). High density maps of V_{CPD} indicate localized region of negative charging in as-deposited film.
2. High - k materials face leakage problems at high fields, similarly BST has current leakage problems at higher voltage. Leakage is only a problem if it perturbs electrical measurements, drains power in instrument implementation of high-k film, causes reliability issues in fielded capacitors due to fluence of charge causing build-up of charged defects which could change operation characteristics (DC bias point) of capacitors.
3. Some parts on the film were non-leaky and CKM provides information on which parts were non-leaky. One of the advantages of this

approach is that one may observe leakage due to change in $V_{CPD}-Q_C$ curves. After each charge deposition the system monitors V_{CPD} for 2.5 seconds with a light pulse between 1 and 1.5 seconds which separates V_D (dielectric voltage) from total V_{CPD} and allows determination of surface barrier and D_{it} (interface trapped charge)..

4. Direct read-out of capacitance values available from dQ/dV values (slope of line) from the graph. Regional changes in slope will be associated with field dependence of capacitance.
5. Capacitance from the plotted graph can provide with the Effective Oxide Thickness (EOT) values which in turn gives k values (with adjustment for leakage). For the present films and thicknesses, k was found to be around 100.
6. The dielectric film (BST) like any other high- k dielectric material shows leakage at high electric fields. Which also depends on the electrode material being used. In our case these films were grown on silicon wafers which has a smaller band offset.

Measurements with Patterned BST Layer by TRL Calibration

The measurement was carried out on polycrystalline alumina (Al_2O_3) samples, which were RF magnetron deposited by $Ba_{0.6}Sr_{0.4}TiO_3$ (300nm). The Ar to O_2 gas ratio was maintained at 90:10. RF power was 200W and in-situ temperature of substrate was $400^\circ C$. After deposition, the samples were

annealed at 900°C for 12 hours in oxygen. Details of the IDC pattern are described in detail in appendix D.

A TRL calibration was used to take S-parameter measurements of devices with a patterned IDC BST layer. Data for devices fabricated on alumina substrates using BST is included. Both 2-port and 1-port devices were measured. The capacitance is extracted at 1 GHz for all devices and biasing conditions using the following expressions:

$$C = -\text{imag}(Y(1,2))/(2*\pi*\text{freq}); \text{ for 2 port devices} \quad (4.2)$$

$$C = \text{imag}(Y(1,1))/(2*\pi*\text{freq}); \text{ for 1 port devices} \quad (4.3)$$

Figure 44 shows the experimental set-up. S-Parameter Measurement specification:

Anritsu 37397 VNA (Lightning) & Cascade Probe Station

GGB 150µm pitch GSG probes

Frequency: 0.04 – 40 GHz

Devices biased up to 90V

Temperature range: 25°C – 125°C



Figure 44. TRL experimental set-up

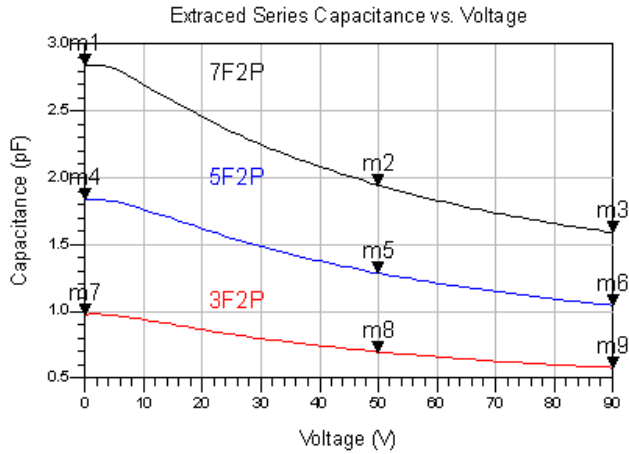
Figure 45 shows the extracted capacitance vs. voltage for alumina samples with their corresponding capacitance at 50 and 90V. The tunability of these films was calculated at 50 and 90V. Average tunability on B5 at 50V was 28.68% and average tunability on B5 at 90V was found to be 40.91%. Figure 46 shows the comparative C-V graph for 3, 5 and 7 finger samples with patterned BST thin films.

Table 7 shows the capacitance extracted for different samples with BST thin film patterns with different annealing ambient gases. The capacitance values shown in the table below were extracted at 1GHz.

Conclusions

The BST thin film structures were seen to have a tunability of 20% at low frequencies and fixed DC biases. The BST thin film structures, which were measured at high frequencies (1GHz) showed a 40% tunability.

Sample B5(Alumina), Best Devices



R8C5_7F2P	R8C3_5F2P	R8C5_3F2P
m1 indep(m1)=0.000 plot_vs(Cs_7F2P,V_dc)=2.843 freq=1.000000GHz	m4 indep(m4)=0.000 plot_vs(Cs_5F2P,V_dc)=1.831 freq=1.000000GHz	m7 indep(m7)=0.000 plot_vs(Cs_3F2P,V_dc)=0.977 freq=1.000000GHz
m2 indep(m2)=50.000 plot_vs(Cs_7F2P,V_dc)=1.943 freq=1.000000GHz	m5 indep(m5)=50.000 plot_vs(Cs_5F2P,V_dc)=1.284 freq=1.000000GHz	m8 indep(m8)=50.000 plot_vs(Cs_3F2P,V_dc)=0.696 freq=1.000000GHz
m3 indep(m3)=90.000 plot_vs(Cs_7F2P,V_dc)=1.588 freq=1.000000GHz	m6 indep(m6)=90.000 plot_vs(Cs_5F2P,V_dc)=1.045 freq=1.000000GHz	m9 indep(m9)=90.000 plot_vs(Cs_3F2P,V_dc)=0.577 freq=1.000000GHz

Figure 45. TRL measurement on alumina BST thin film sample

The CK-M measurements were conclusive in understanding the leakage characteristics of the BST dielectric thin films. There is clearly a relationship between the crystal orientation of the films and their electrical behavior. It can be concluded that, the BST films with random crystal orientation (sol-gel) and a combination (stacked) possess the ability to withstand higher voltage as compared to uniform crystallinity (sputtered). This could be due to the presence of aligned grain boundaries in the film structure that provide a path from top surface to bottom for the current to

flow, such as the columnar structure in sputtered films. A combination of deposition processes, such as that of stacked films, provides for a mismatch in between the sputtered and sol-gel layer leading to a non-continuous pathway for current to flow hence, it can sustain higher potentials.

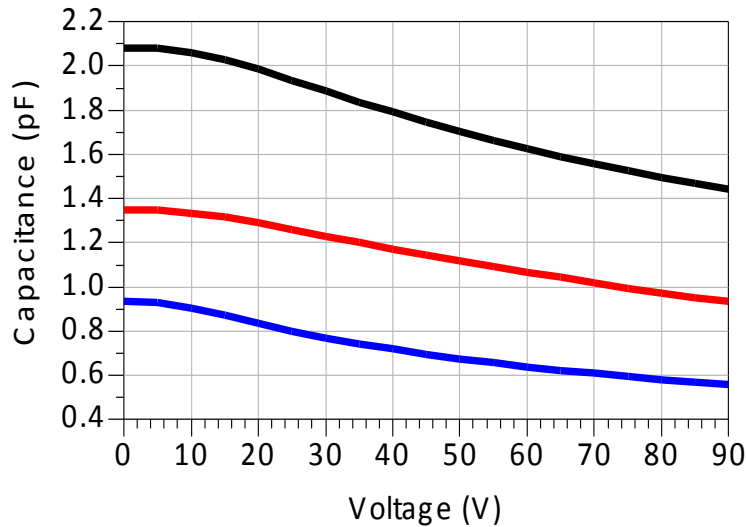


Figure 46. TRL measurement of blue - 3 finger IDC pattern, red - 5 finger IDC pattern and black - 7 finger IDC pattern on BST deposited alumina substrate

Table 7. Capacitance values extracted at 1GHz for different devices fabricated on alumina substrates

Device Name	Capacitance at 0 V (pF)	Capacitance at 50 V (pF)	Capacitance at 90 V (pF)
B3_R2C1_5F2P	1.709	1.152	0.940
B3_R3C3_7F2P	2.604	1.861	1.531
B3_R6C3_5F2P	1.758	1.258	Not Available
B3_R6C5_7F2P	2.820	1.934	1.567

Table 7. (Continued)

Device Name	Capacitance at 0 V (pF)	Capacitance at 50 V (pF)	Capacitance at 90 V (pF)
B3_R6C7_7F2P	2.775	1.898	Not Available
B5_R6C3_5F2P	1.831	1.284	1.045
B5_R6C5_7F2P	2.843	1.943	1.588
B5_R6C7_7F2P	2.646	1.854	1.524
B5_R7C4_7F1P	-1.60e-4	2.22e-4	3.43e-4
B5_R7C7_5F2P	1.734	1.240	1.026
B5_R8C5_3F2P	0.977	0.696	0.577
B5_R8C6_3F1P	1.96e-5	-4.88e-6	5.18e-5
B5_R8C7_3F2P	0.936	0.675	0.560
B7_R1C5_3F2P	0.904	0.681	0.558
B7_R2C5_7F2P	2.314	1.767	Not Available
B7_R2C6_7F1P	3.34e-4	-9.78e-5	1.51e-4
B7_R3C3_7F2P	2.048	1.639	1.394
B7_R4C3_5F2P	1.369	1.112	0.941
B7_R4C5_3F2P	0.797	0.636	0.544
B7_R6C3_5F2P	1.288	1.076	0.915
B7_R6C7_7F2P	2.031	1.627	1.371
B7_R7C6_5F1P	5.46e-5	4.45e-5	2.05e-4

Table 7. (Continued)

Device Name	Capacitance at 0 V (pF)	Capacitance at 50 V (pF)	Capacitance at 90 V (pF)
B7_R8C6_3F1P	1.78e-4	2.39e-4	1.48e-4
B10_R2C6_7F1P	3.15e-4	3.67e-5	0.002
B10_R3C7_5F2P	1.347	1.117	0.934
B10_R6C5_7F2P	2.080	1.701	1.442
B10_R7C7_5F2P	1.379	1.079	0.910
B10_R8C5_3F2P	0.654	0.520	0.446
B10_R8C7_3F2P	0.656	0.511	0.433

Chapter 5: Application of BST in Graphene Conducting Polymer

Supercapacitor Electrode

Introduction to Energy Storage Devices

Supercapacitors are a family of energy storage devices which belong to electrochemical capacitors. Conventionally, energy storage has been achieved using electrostatic capacitors, electrolytic capacitors, batteries, fuel cells and electrochemical capacitors. These devices have various applications depending on their energy and power storage capability. Supercapacitors are sometimes termed also as ultracapacitors or electrochemical double-layer capacitors (EDLC). Table 8 summarizes the performance of different energy storage devices available in the market [125]. Even though batteries can store large amount of energy, they fall short in the cycle life area due to Faradaic processes. In EDLCs, the charging and discharging does not involve any chemical or compositional changes, it is governed by just an exchange of electrons between the cathode and anode. Due to the high demands in recent applications, like smart phones, satellite communication devices, high-end PCs and automobiles, standard batteries are proving incapable to fulfill the requirements. This has driven the market to design special high-power, long life cycle pulse batteries.

Table 8. Comparison between basic characteristics of batteries, capacitors and supercapacitors

Parameter	Battery	Capacitor	Supercapacitor
Charging time	0.3-3 hrs	$10^{-6} - 10^{-3}$ s	1-30s
Discharge time	1-5 hrs	$10^{-6} - 10^{-3}$ s	1-30s
Energy density (Wh/kg)	20-100	<0.1	1-10
Power density (W/kg)	~50-200	>10000	~1000-2000
Life cycle	~500-2000	>500000	>100000
Charge/discharge efficiency	~0.7-0.85	~1.0	~0.9-0.95
Operating voltage (V)	1.25 to 4.2/cell	6 to 800	2.5 to 3
Operating temperature (°C)	-20 to 65	-20 to 100	-40 to 85

Figure 47 [144] illustrates the fixed capacitors charge storage principles. Supercapacitors can be considered as a bridge between conventional capacitors and rechargeable batteries. They have the highest available capacitance values per unit volume and the greatest energy density of all capacitors [126]. "Power density is defined as the product of energy density, multiplied by the speed at which the energy is delivered to the load" [125]. The greater power density results in much shorter charge/discharge cycles than a battery is capable, and a greater tolerance for numerous charge/discharge cycles.

In the electrochemical capacitors, the electrolyte constitutes the conductive connection between the two electrodes, distinguishing them from electrolytic capacitors, in which the electrolyte only forms the cathode, the second electrode. Supercapacitors are polarized and must operate with correct polarity. Polarity is controlled by designing the electrodes symmetrically (potential applied) or asymmetrically (designed).

Supercapacitors find applications in a broad spectrum of commercial devices for power and energy requirements, such as:

- Low supply current during longer times for memory backup in (SRAMs)
- Power electronics that require very short, high current, as in the KERSsystem in Formula 1 cars
- Recovery of braking energy for vehicles

The capacitance value of an electrochemical capacitor is determined by two storage principles, which contribute to the total capacitance [127-129].

- Double-layer capacitance: “electrostatic storage of the electrical energy achieved by separation of charge in a Helmholtz double layer at the interface between the surface of a conductive electrode and an electrolyte” [125].

Fixed capacitors, charge storage principles

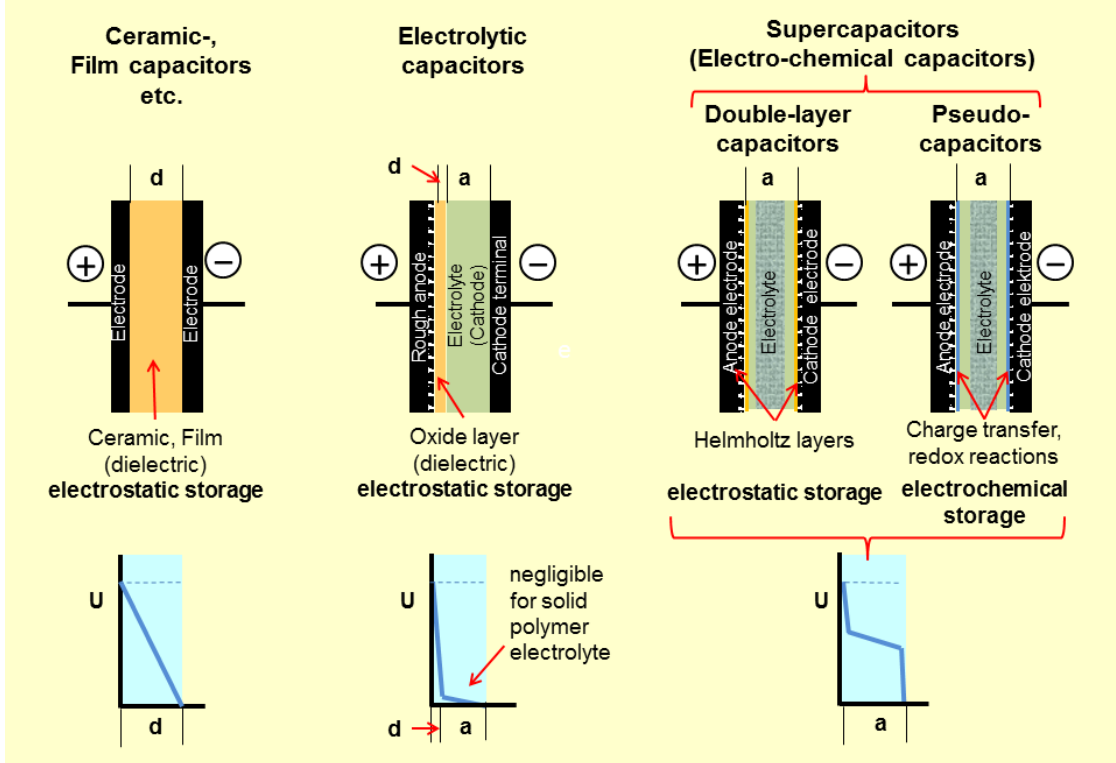


Figure 47. Conventional electrostatic vs. electrochemical energy storage [144]

- Pseudocapacitance: "electrochemical storage of the electrical energy with electron transfer, achieved by redox reactions with specifically adsorbed ions from the electrolyte, intercalation of atoms in the layer lattice or electrosorption, underpotential deposition of hydrogen or metal adatoms in surface lattice sites which result in reversible faradaic charge-transfer" [130].

Conventional supercapacitors are divided into 3 families, based on the design of the electrodes:

- Double-layer capacitors – with carbon electrodes or derivatives with much higher static double-layer capacitance
- Pseudocapacitors – made of metal oxide or conducting polymer electrodes
- Hybrid capacitors – asymmetric electrodes made from both conducting polymer double-layer and metal oxide electrodes.

Pseudocapacitance properties can be expressed using a cyclic voltammogram. Ideally, for a double-layer capacitor the sign of the current changes immediately as you reverse the potential and the shape of the voltammetry is rectangular. Figure 48 [145] depicts the cyclic voltammetry between an ideal capacitor and a supercapacitor with pseudocapacitance.

The current is independent of the potential of the electrode for electrostatic type of energy storage devices. For double-layer capacitors (EDLCs), the shape of the graph changes to that of a parallelogram. For electrodes showing pseudocapacitance, the charge stored in the capacitor is strongly dependent on the potential of the electrode. Therefore, there is a shift in the voltammetry characteristic from the parallelogram, which is brought in by the delay of potential during reversing of the potential, coming into picture due to the kinetic processes during the charging of the pseudocapacitor [126, 131].

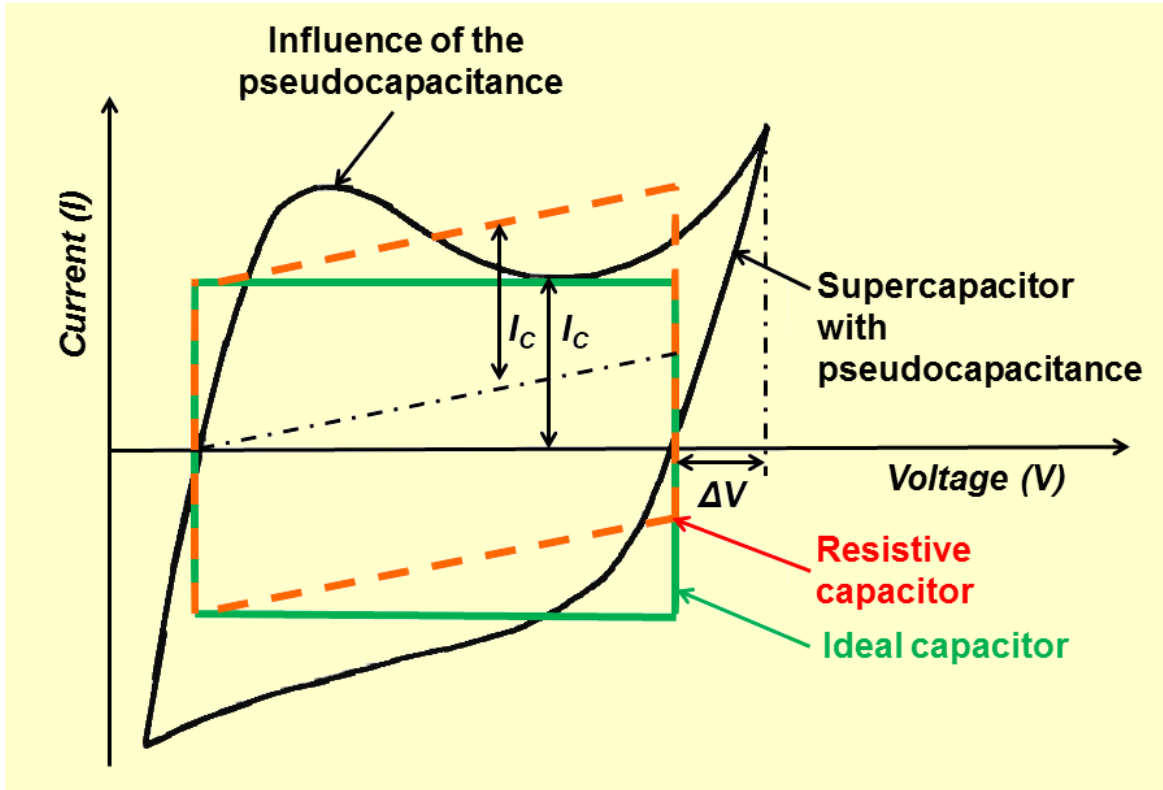


Figure 48. Cyclic voltammogram difference between an ideal capacitor and a supercapacitor with pseudocapacitance [145]

Electrochemical capacitors, which have high pseudocapacitance, have two major advantages over batteries: charging and discharging of electrochemical capacitors is much faster than in batteries almost as fast as conventional capacitors and the cycle lifetime is much higher than that of batteries.

Introduction to Carbon-based Supercapacitors

Carbon-material and in particular, graphene has attracted significant attention in the scientific community due to its superior electronic, physical and mechanical properties pertaining to high energy storage applications.

For this report, graphene (G)-polyaniline (PANI) was synthesized and used as an electrode to study its electrochemical properties. A leakage current due to the Faradic reactions at the surface of the electrodes hinders the effective use of GPANI electrodes in supercapacitor applications. Coating the surface of the GPANI electrodes with a thin film of a dielectric material generates a potential barrier, which reduces the reaction rate with a slight drop in specific capacitance but increases the relative dielectric constant by increasing the capacitance of the supercapacitor and at the same time reducing the leakage current.

Carbon-material based electrodes are the most popular candidate for energy storage application because of their desirable physical and chemical properties. There have been several attempts to incorporate graphene with other pseudocapacitance materials for use in supercapacitors. This investigation proposes that coating the surface of Graphene-polyaniline electrodes with a dielectric material such as Barium Strontium Titanate (BST) will enhance the electrical properties of the electrochemical double layer cell. The BST will not only inhibit the leakage current, but also provide isolation for the GPANI electrode. High conductivity, wider tunable potential window, stability of the electrode material in doped form, faster charge transfer rate, short charging times in graphene-conducting polymer and dielectric layer on Graphene-conducting polymer will allow for fabricating and designing a high performance supercapacitor. The overall idea is to

incorporate the superior properties of various G-conducting polymer composites with BST. Figure 49 depicts the molecular structure of graphene and other polymer base units, which are used in conjunction with graphene.

Table 9 summarizes the specific capacitance values for carbon-based supercapacitors (data collected from different journal articles).

Table 9. Specific capacitance values for carbon-based supercapacitors

Material	Capacitance
Nomex-derived activated carbon fibers [132]	175 F/g (5.25 M sulfuric acid)
Carbon Aerogel [133]	46 F/cm ³ (30% H ₂ SO ₄ Method: Charging-discharging two-electrode configuration)
Carbon black [134]	250 F/g (3M H ₂ SO ₄ Three-electrode configuration)
Printable Thin Film SWCNTs[135]	35 F/g (LiPF ₆ /EC:DEC, two-electrode configuration)
Graphene [136]	117 F/g (1M aq. H ₂ SO ₄) 75 F/g (PYR14TFSI Ionic liquid)

For the present investigation, commercially available nano-sized graphene from Angstrom technologies was used. Polyaniline was synthesized from commercially available aniline monomer. A prototype electrochemical cell built by the process described in the following sections is shown in Figure

50.

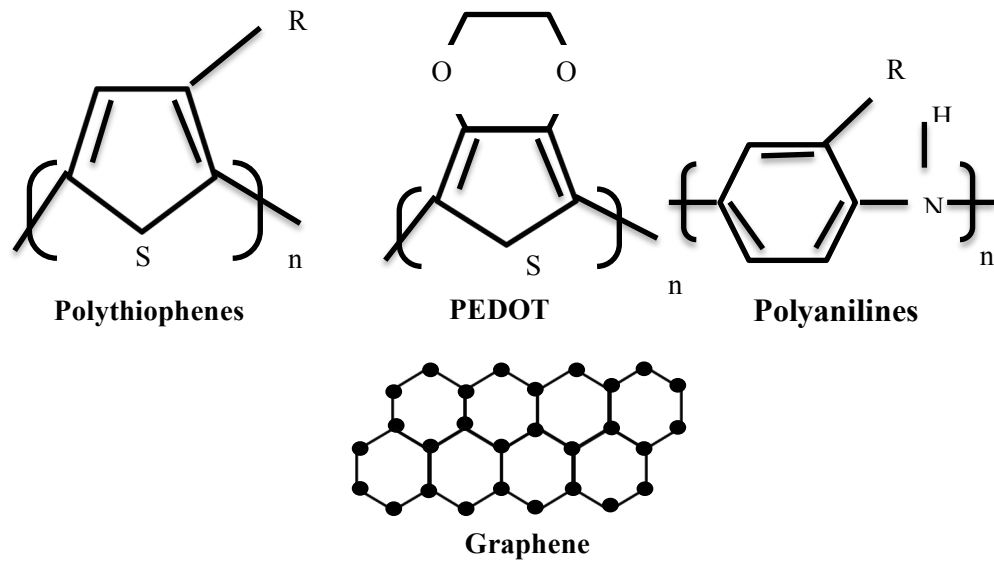


Figure 49. Structure of graphene and few conducting polymeric materials [137]

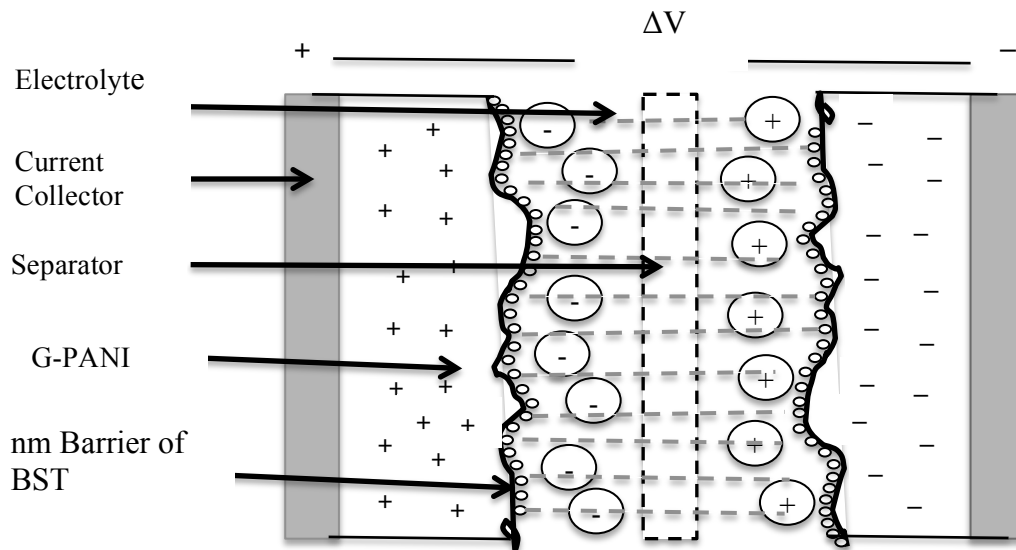


Figure 50. Schematic of prototype supercapacitor [143]

Experimental

Three different types of symmetric electrode cells for supercapacitor applications were prepared and their properties were electrochemically investigated. The following sections give a brief description of how the electrochemical cells were prepared.

Graphene-Polyaniline (GPANI) Electrode (Standard or Control)

The GPANI solution was drop-coated on graphite substrates and dried at 100°C. Figure 51 displays the photograph of the electrochemical set-up used for our experiments.

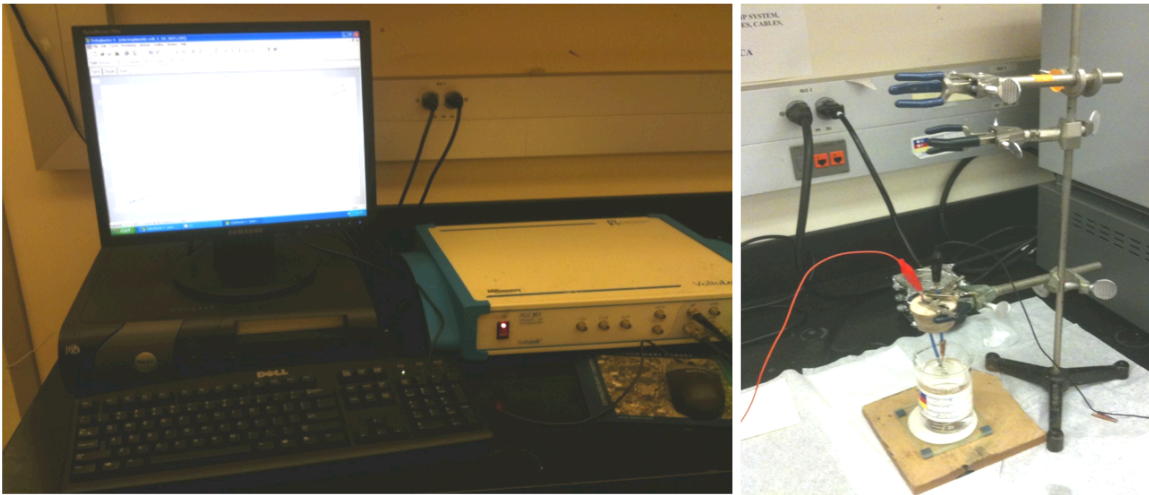


Figure 51. Photograph of a typical electrochemical set-up available in our facility

Graphene-Polyaniline (GPANI) Coated with Sol-gel BST Electrode

The GPANI electrodes prepared, as described above, were dipped in a BST sol-gel solution. The 'electrophoresis' approach was adopted to deposit BST nanoparticles on the GPANI coated graphite substrate [138]. Figure 52 illustrates the process of electrophoresis for our deposition.

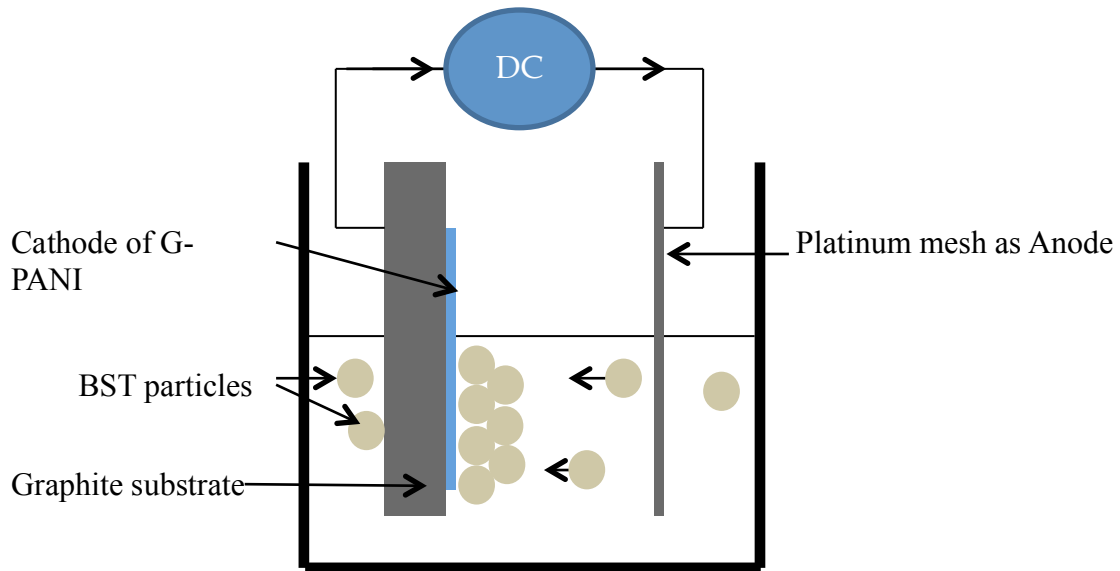


Figure 52. Schematic of electrophoretic deposition of BST from sol-gel solution

Graphene-Polyaniline (GPANI) Coated with Sputter Deposited BST Electrode

A few of the GPANI electrodes prepared were sputter deposited with BST as an alternate preparation approach to the electrophoretic method above. An RF magnetron sputtering system, CMS-18, was used for sputtering a very thin layer of BST, few tens of nanometers, on the GPANI substrates at room temperature. Details pertaining to the sputtering system deposition procedure are described in the previous chapter.

Results

SEM of GPANI and GPANI+BST Electrodes

Figure 53a and b shows SEM micrographs of GPANI+sol-gel BST and GPANI+sputter deposited BST electrodes, respectively. SEM shows particles

on the GPANI+sol gel BST (a) and GPANI+sputter BST (b) electrode surfaces suggesting a non-uniform or clustered deposition of BST.

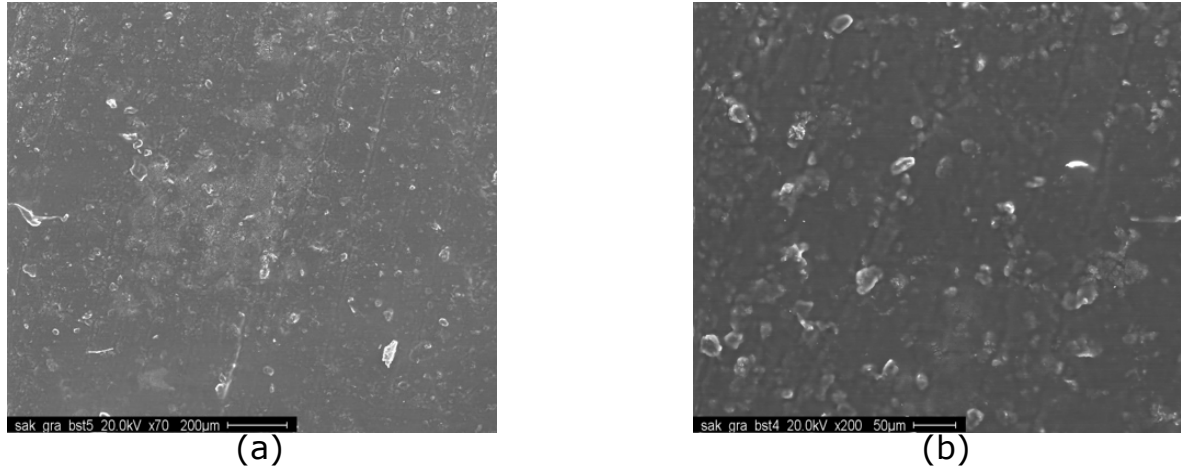


Figure 53. SEM micrograph of a) GPANI sol-gel BST electrode and b) GPANI sputter deposited BST electrode

Comparative Cyclic Voltammetry Studies of GPANI, GPANI+sol gel BST and GPANI+sputter Deposited BST in 2M H₂SO₄

Cyclic voltammetry experiments were carried out on the GPANI and GPANI+BST electrodes in 2M H₂SO₄ electrolyte. The responses for these electrode cells are illustrated in figure 54. The CV plots are different in response relative to the original GPANI electrode cell. Figure 53 compares the CV of GPANI standard electrode cell and GPANI+sputter BST electrode cell. It is clear from the graph that the capacitance window of the GPANI+sputter BST is diminished compared to that of the GPANI electrode cell. This could be due to the reduction of surface area available for holding charge on the GPANI sites.

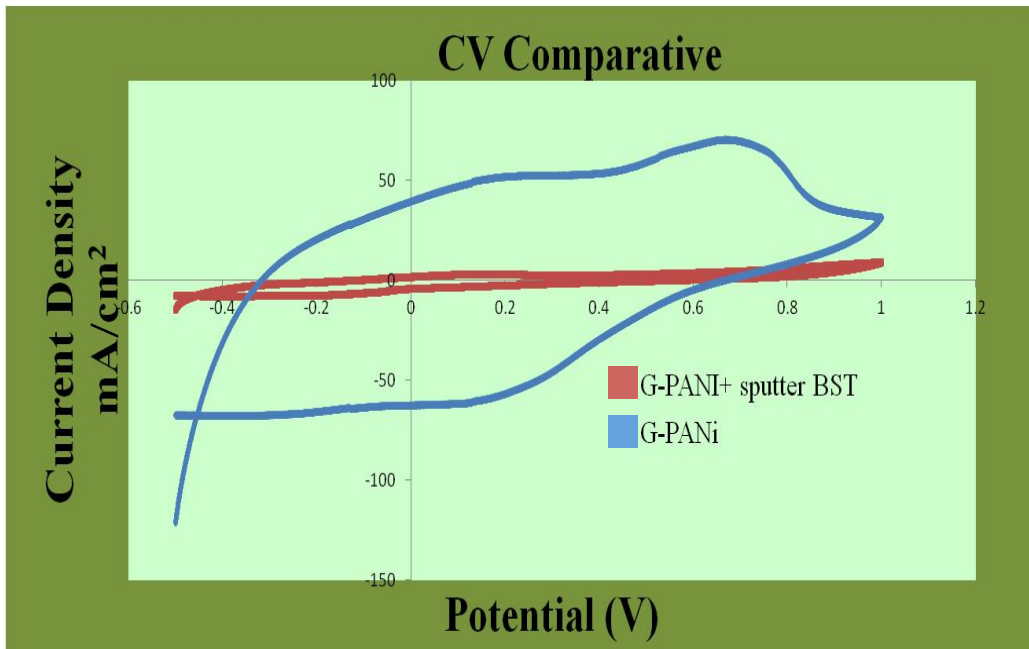


Figure 54. Current density vs potential response of GPANI and GPANI+BST sputter electrodes at a scan speed of 5mv/s

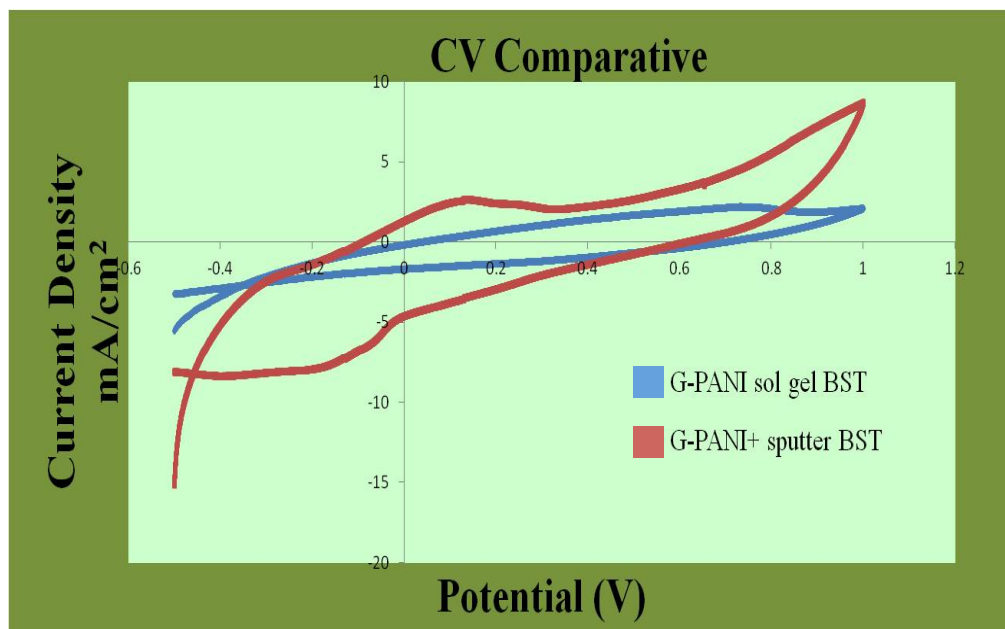


Figure 55. Current density vs potential of GPANI+BST sol gel and GPANI+BST sputter electrodes at a scan speed of 5mv/s

A comparative graph between GPANI+sol gel and GPANI+sputter BST electrode cells is illustrated in Figure 55. The response of GPANI+sputter BST is better than that of GPANI +sol gel BST electrode. The GPANI+sputter electrode cell is able to hold more charge as compared to that of GPANI+sol gel. This could be the result of better coverage of the GPANI layer with BST film, sputtering being a more uniform method of deposition.

Comparative Charging and Discharging Studies of GPANI, GPANI+BST Sol gel and GPANI+BST Sputter Electrodes

Charging-discharging responses of the three different electrode structures investigated in this work are presented in figure 56. The GPANI+sputter BST electrode cell response is the most significant. The GPANI+sputter electrode cell charges to a higher potential compared to the other two structures. Further, the decay evident in the GPANI characteristic is absent in the GPANI+sputter electrode characteristics. The GPANI electrode cell charging and discharging characteristic shifts to increasing negative potential bias as a function of cycle order. In comparison, the structures incorporating the GPANI+sol gel electrode are not as symmetrical as the GPANI+sputter electrode, but also exhibits no significant negative bias. Analysis shows that BST layers display little if any trend in negative bias. This suggests the possibility that BST may be acting as a protective layer inhibiting the leakage of charges over time and preventing the permanent alteration of the GPANI redox state.

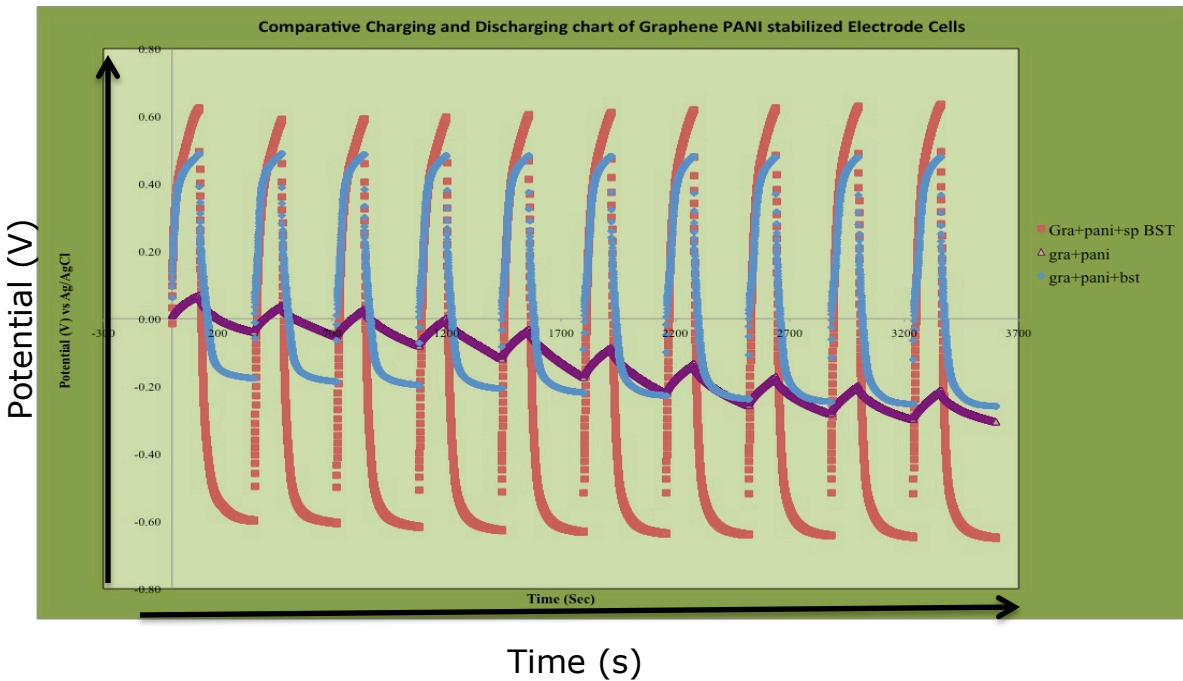


Figure 56. Potential vs time response of GPANI (purple), GPANI+BST sol gel (blue) and GPANI+BST sputter (red) electrodes for charging and discharging

Conclusions

Dielectric films of BST were successfully deposited over GPANI electrodes using electrophoretic and sputtering techniques. BST layers significantly alter the CV response of capacitor structures where they have been added as a separator layer over existing GPANI films. Charging and discharging responses of capacitors with BST incorporation appear more stable and exhibit higher potential ranges than GPANI supercapacitor structures.

Chapter 6: Graphene-Polyaniline-BST Composite Symmetric Electrodes in Supercapacitor Application

Introduction

The electrochemical capacitors are electric energy storage devices that are used in transportation and portable electronic applications because they have higher power densities than rechargeable batteries, but higher energy than conventional capacitors. Recently, supercapacitors from highly conducting nanocomposite materials were fabricated by chemically synthesizing graphene (G)-polypyrrole (PPY), G-polyaniline (PANI), G-polyethylenedioxythiophene (PEDOT) and G-polythiophene (PTH) conducting nanocomposite materials [140-142]. The issue of leakage current on graphene-polyaniline by depositing barium strontium titanate (BST) dielectric layer through electrophoretic and sol-gel techniques [143] has been addressed in the earlier chapter. This chapter focuses on incorporating BST molecules in the GPANI polymer matrix during the preparation of GPANI. This is done to understand the molecular interactions between GPANI and BST, and further understand and study the effect on the electrochemical properties of GPANI+BST electrodes. The incorporated BST structure is termed as M&M structure because it encapsulates GPANI molecules. It was

found that the specific capacitance of these electrodes improved from 100F/g for GPANI electrodes to 540F/g for GPANI+BST electrodes. The work intends to understand the leakage behavior of the electrodes using diffusion coefficient.

The films were characterized using scanning electron microscopy (SEM), X-ray-diffraction (XRD), electrochemical impedance spectroscopy (EIS) and cyclic voltammetry (CV) techniques. These techniques were used to compare the specific capacitance, charging discharging, stability and life cycle of supercapacitor electrodes fabricated using graphene-polyaniline-BST nanomaterials.

Motivation

Figure 57 illustrates the motivation behind this work. The main aim was to improve on the electrochemical properties of GPANI electrochemical electrodes for supercapacitor applications. Since in the previous chapter we have already established an improvement in the leakage properties of the electrodes by depositing a thin BST layer on these GPANI electrodes, the only logical next step was to incorporate BST molecules in the GPANI polymer matrix.

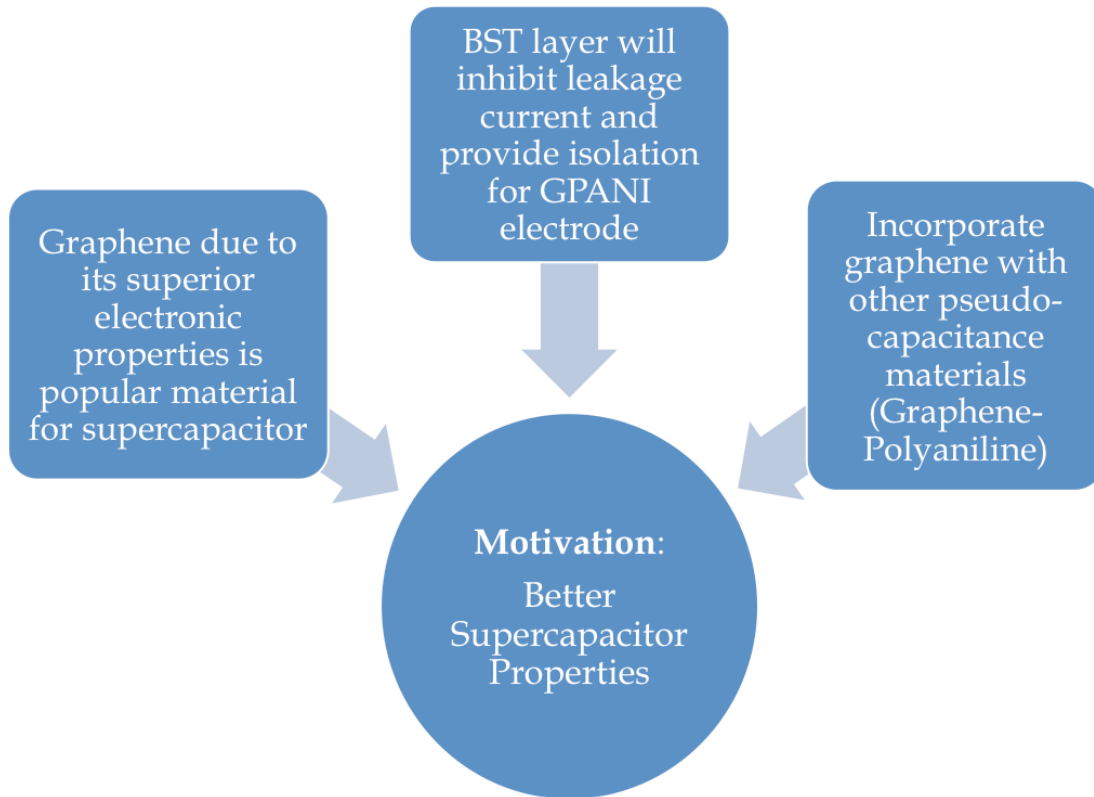


Figure 57. Motivation for the present investigation

Goals

- Coating the surface of BST on GPANI will generate a barrier, which will reduce the reaction rate with a slight drop in the specific capacitance.
- The supercapacitor will display low leakage current due to the presence of a BST layer on the GPANI nanomaterial film.
- The supercapacitor will behave like a rechargeable battery, which means that the supercapacitor will possess a better specific capacitance as compared to a simple GPANI-based supercapacitor.

Experimental

Incorporated BST functional molecules within the Graphene Polyaniline synthesis step. Chemically formed a M&M structure with GPANI as the center and BST as outer shell. Figure 55 illustrates the proposed molecular structure of the GPANI+BST composite matrix.

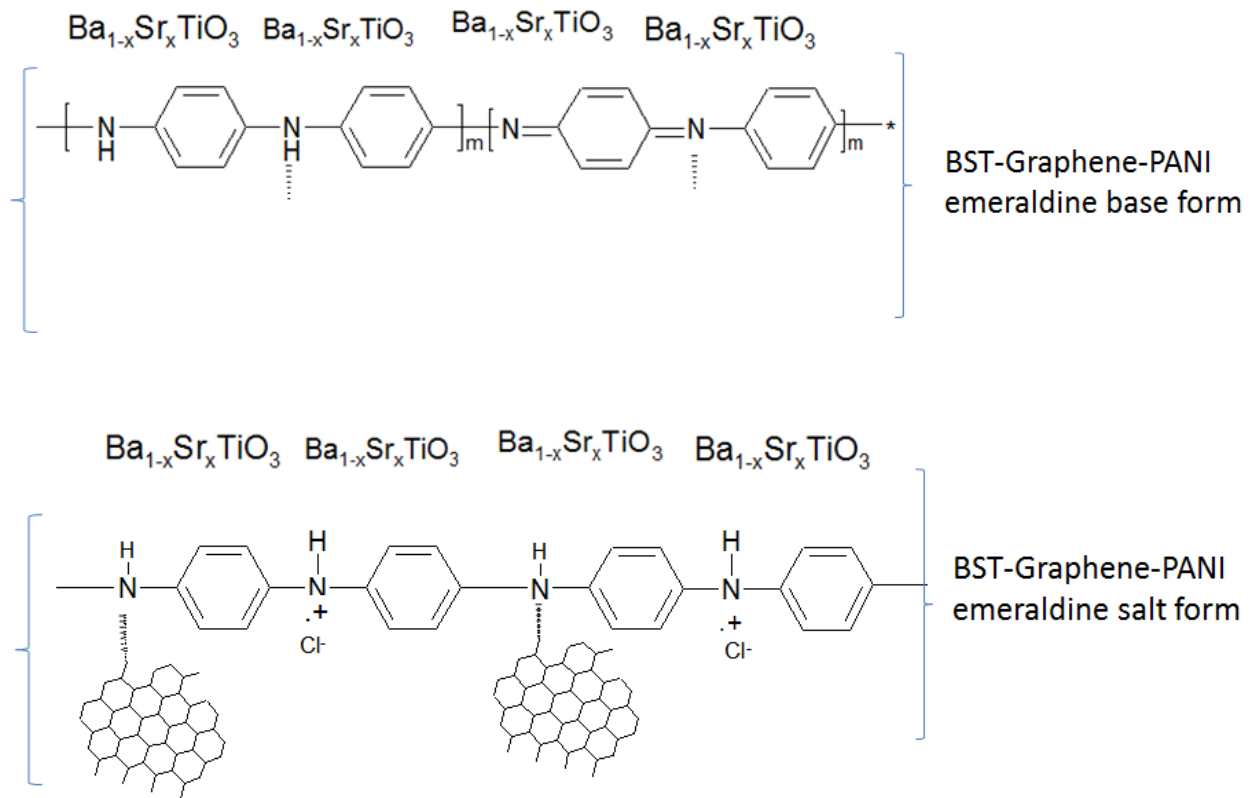


Figure 58. Molecular proposed structure of the GPANI+BST composite matrix in both emeraldine base and emeraldine salt (doped) states

Results

SEM of GPANI and GPANI BST Electrodes

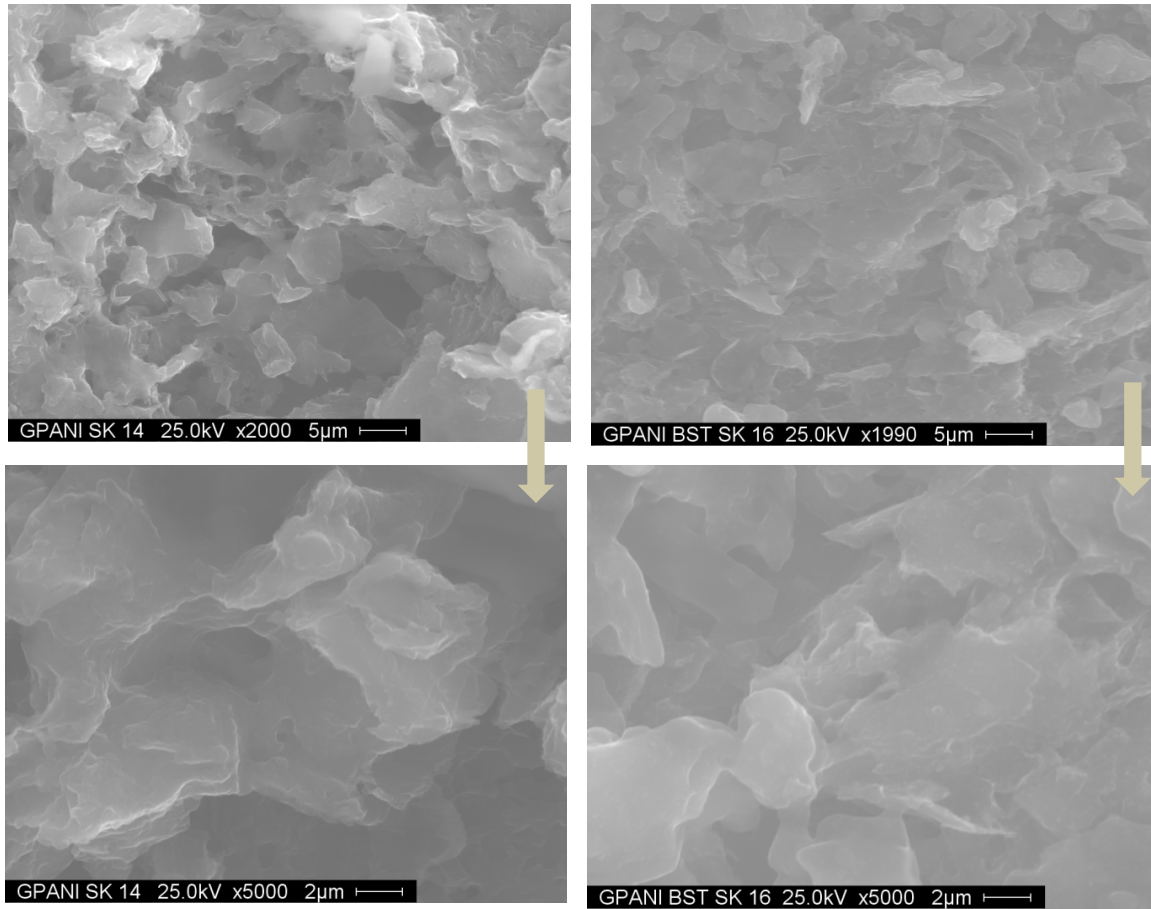


Figure 59. SEM micrographs of GPANI BST structures

The SEM pictures depicted in the adjacent figure 56 taken at 500X magnification illustrate the presence of a thin layer of BST and porous structure. This SEM picture shows typical plate-like characteristics of GPANI-based material.

XRD of GPANI and GPANI+BST Electrodes

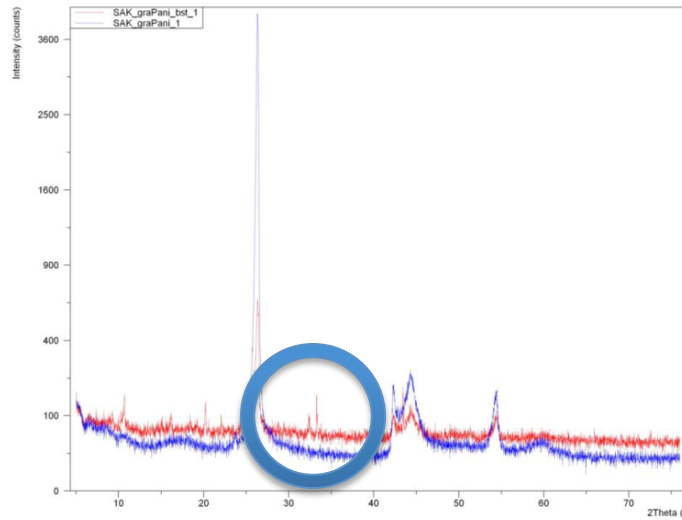


Figure 60. Comparative XRD of GPANI and GPANI BST electrodes

The XRD in the given figure 57 shows a few extra peaks, which correspond to BST on the GPANI electrode (circled). Figure 57 (red curve) shows the characteristic GPANI with BST at 2θ of 32° . Blue shows characteristic peaks for GPANI.

Comparative Cyclic Voltammetry Studies of GPANI, GPANI+BST Processed and GPANI+BST NMP Processed Electrodes

Figure 60 shows the cyclic voltammetry of symmetric graphite/GPANI, graphite/GPANI+BST (doped powder) and graphite/GPANI+BST (N-methyle 2 pyrrolidone) symmetric electrodes supercapacitor in 2M H_2SO_4 . The graphite /GPANI electrode shows redox peak at 0.8V whereas there is a shift in the redox peak for GPANI+BST fabricated using BST powder or NMP film.

The BST layer is able to control the oxidation and reduction process of the GPANI composite material. The CVs studied in all three supercapacitor reveal

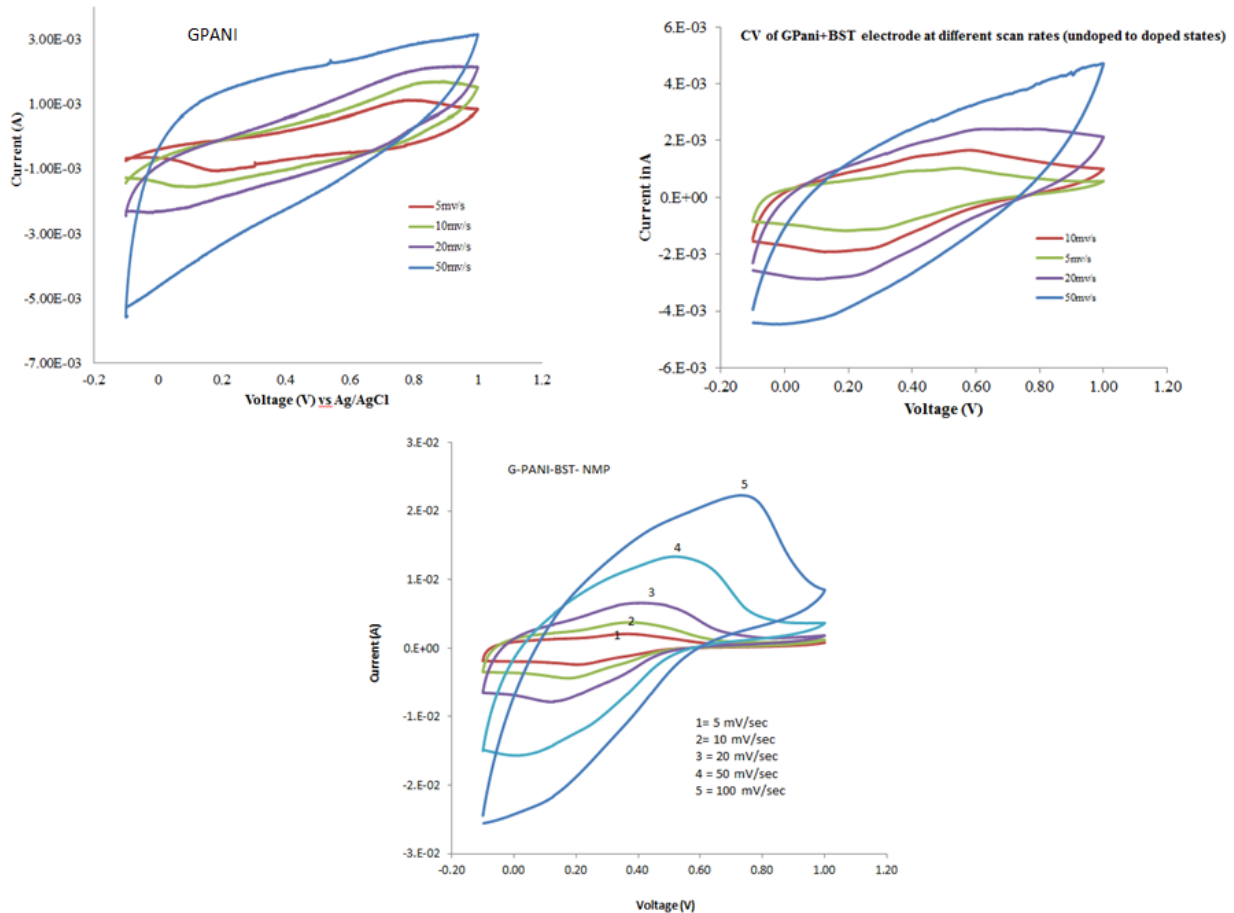


Figure 61. Cyclic voltammetry of GPANI, GPANI+BST (doped) and GPANI+BST (N-methyl 2 pyrrolidone)

that the system is diffusion controlled. The coating over GPANI shows better regulation than simple GPANI electrode. We have made an attempt to calculate the specific capacitance at different scan rates. The specific capacitance has been calculated using the equation,

$$C = i / (m \times \Delta V / \Delta t) \quad (5.1)$$

where, i is the average current in the redox process and $\Delta V / \Delta t$ is the scan rate and m is the mass of the electrode material. The capacitive effect of graphite electrode has been neglected in this study. The GPANI electrode shows average specific capacitance of 93 - 100 F/g where as the GPANI+BST electrode shows specific capacitance of 500 - 540 F/g. The effect of BST is clearly distinguished in the capacitor indicating that the BST film formed is able to increase the double layer capacitance in GPANI+BST based supercapacitor. Further, the diffusion coefficient of GPANI and GPANI+BST has been calculated using Randles Sevcik equation.

Randles- Sevcik equation is given by,

$$I_p = (2.69 \times 10^5) \cdot n^{3/2} \cdot A \cdot D_f^{1/2} \cdot C_0 \cdot V^{1/2}, \quad (5.2)$$

where D_f is the diffusion coefficient, I_p is the current peak in CV, n represents number of electrons, A is the area of the electrode, and C_0 is concentration of the H_2SO_4 electrolyte which is equal to 2. Difference in diffusion coefficient corresponds to difference in leakage current.

The calculated Diffusion coefficient is given by,

- $0.73 \times 10^{-12} \text{ m}^2/\text{s}$ for GPANI electrodes
- $1.09 \times 10^{-12} \text{ m}^2/\text{s}$ for GPANI+BST electrodes

Comparative Charging and Discharging Studies of GPANI, GPANI+BST Processed and GPANI+BST NMP Processed Electrodes

Charging discharging over 10 cycles is shown in figure 61. The GPANI+BST electrodes maintain their shape for the 10 cycles. Charging and discharging curves are uniform for GPANI, GPANI+BST processed and GPANI+BST NMP based electrodes. Faradaic exchange of ionic charge in GPANI+BST electrodes causes the peculiar uniform charging-discharging. GPANI+BST charges to higher potential as compared to GPANI electrodes. Interestingly, GPANI+BST electrodes show a higher potential difference for charging and discharging at $1\text{mA}/\text{cm}^2$.

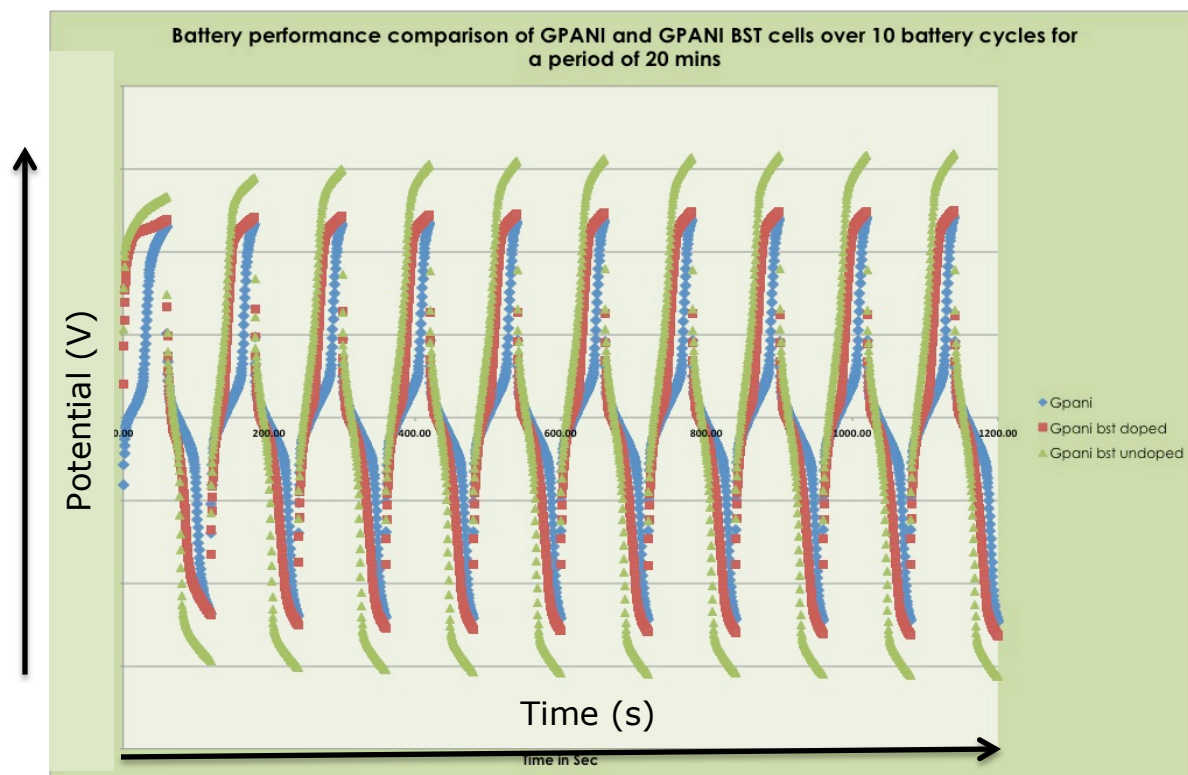


Figure 62. Charging discharging for 10 cycles GPANI, GPANI+BST processed and GPANI+BST NMP electrodes

Comparative EIS Studies of GPANI, GPANI+BST Processed and GPANI+BST NMP Processed Electrodes

Figure 62 shows the Nyquist plot of GPANI, GPANI+BST processed and GPANI+BST NMP. The GPANI electrode shows a typical Nyquist plot with internal resistance being 6 ohms at a higher frequency. The typical space charge effect or battery effect could be observed at lower frequencies.

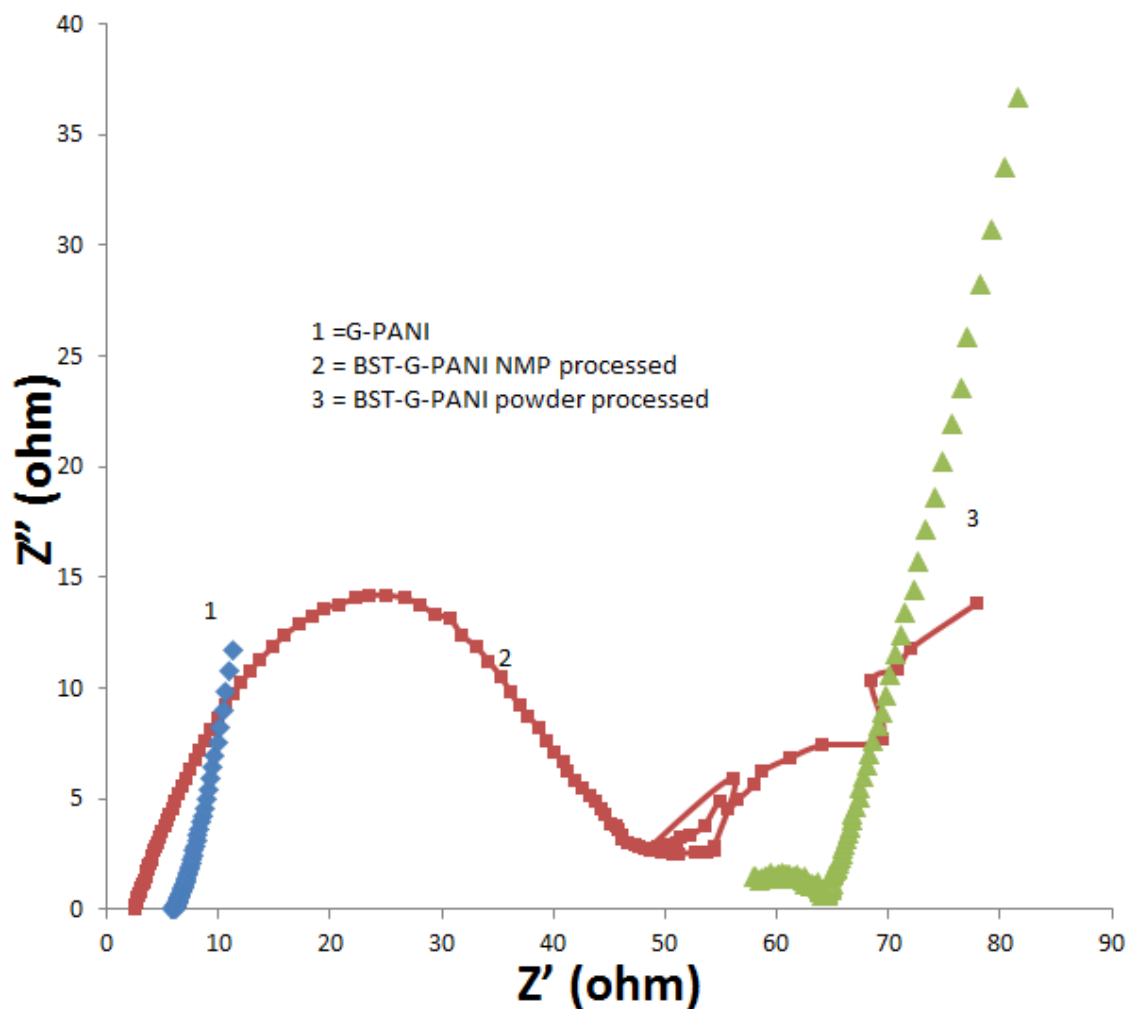


Figure 63. Nyquist plot of GPANI, GPANI+BST processed and GPANI+BST NMP symmetric supercapacitor electrodes in 2M H_2SO_4 electrolyte

GPANI+BST NMP processed electrodes display an internal resistance of around 3 ohms besides the typical dielectric behavior due to the presence of BST in GPANI composite. However, the powder processed GPANI+BST shows an internal resistance of 63 Ohms, a much higher value than either NMP processed GPANI+BST or GPANI-based electrode systems.

Conclusions

Electrochemically symmetric supercapacitors based on GPANI+BST NMP processed and GPANI+BST powder processed were fabricated. The thin BST layer on GPANI has been found to play a critical role in improving the specific capacitance value of supercapacitors. The GPANI+BST based symmetric supercapacitor showed a specific capacitance of 500 - 540 F/g in comparison to 93 - 100 F/g for GPANI based the supercapacitor.

Chapter 7: Conclusions and Future Work

Conclusions

The central idea behind this investigation is to understand the role of BST thin film growth on various substrates and relate it to its electrical and electrochemical behavior. Depending on the process and application, BST thin films trap charges by inhibiting leakage.

The structural and electrical properties of RF magnetron sputtered, sol-gel process and 'stack' process have been compared. It has been established that the electrical performance of 'stacked' films is better than that of the individual ones.

Corona-Kelvin metrology has been employed to study the leakage behavior of the deposited films and compare their properties based on the charge they can retain or the voltage that these films can hold. It has been established that voltage of above 25V positive and negative can be applied to these films without dielectric layer damage or leakage.

Use of GPANI with BST enhances the electrochemical properties of the conducting polymer for superconductor applications. A positive improvement

in the charging and discharging times has been achieved for GPANI+BST electrodes as compared to GPANI electrodes.

A simple but effective approach of introducing BST dielectric molecules in the GPANI solution was carried out and the electrode results were compared with GPANI electrodes. The fabricated electrodes (with BST) showed superior electrochemical properties as compared to GPANI electrodes. There is a substantial increase in the diffusion coefficient suggesting a controlled exchange of charges. The EIS studies show that the resistance component for GPANI+BST electrodes is higher than that for GPANI electrodes, suggesting that the BST layer avoids the leakage current.

Future Work

Comparative stress induced studies of BST thin films deposited by different methods (sputtering, sol-gel and 'stacked') needs attention. This study will be useful in understanding the role of the substrate and its effect on the crystallinity of the BST thin film layer. This, in turn, will be used for determining the relationship between the crystallinity and the leakage behavior.

Compare trap assisted leakage mechanism in sputtered and sol-gel films. A thorough study of trap-assisted leakage mechanism should be carried out to understand the role of deposition methods on the leakage behavior of the BST thin films.

Other deposition processes like Langmuir-Blodgett can be employed to deposit BST on GPANI electrode cells and their behavior with respect to thickness variation can be studied. For the current investigation it was not possible to vary the thickness in a uniform and controlled manner. This hurdle can be overcome by use of a different technique.

For supercapacitor application study, longer duration charge leakage studies need to be carried out. The duration of charging needs to be extended to 4hrs and discharging to more than 12hrs to understand the effect of charge recombination.

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Author	J. Robertson, C. W. Chen
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Appendix A (continued)

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to Tony, Tony ▾




Tony,

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Consider this as a formal email to use it with proper referencing and changes made with respect to my films.

Thanks for your help

Regards




...

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to Tony ▾

thanks Tony.
Help, permission and quick response appreciated.

...

Appendix A (continued)

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Appendix A (continued)

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--
Supriya Ketkar
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Mukherjee, Devajyoti <dmukherj@usf.edu>
To: "Ketkar, Supriya" <sketkar@mail.usf.edu>

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Dev

Devajyoti Mukherjee, Ph. D.
Postdoctoral Research Associate
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Appendix B Working Principle and Sputtering Guideline for Using CMS-18 RF Magnetron Sputtering System to Deposit BST

Sputtering is a physical vapor deposition (PVD) process, where atoms from a target (Pt, Cu, etc.) are ejected by high energy ion bombardments and deposited onto a substrate. After the vacuum chamber is evacuated a sputtering gas, typically argon, is introduced into the chamber. Several kilovolts of dc bias is applied to the negative terminal of the magnetron gun, which accelerates the electrons towards the anode. The electrons follow a cycloidal path on the cathode with the applied magnetic field and collide with argon atoms. An electron with high enough energy can knockout an electron from argon converting it into a positively charged ion (Ar^+). Then, the positive Ar^+ ions are driven to the cathode where they collide with the target atoms and eject (sputter) them through momentum transfer. The plasma is initiated by the multiplication of these collisions. The chamber pressure is usually kept at between 5-50 millitorrs during sputtering. After a visible plasma is obtained it is observed that a current flows and the target material is deposited onto the surfaces with potential higher than that of the cathode (i.e. substrate, chamber walls). This dc discharge is sustained due to the generation of ion-induced secondary electrons at the cathode.

If an insulating material is used as the target material, a practically impossible amount of dc voltage ($\sim 10^{12}$ V) is needed to achieve the same current density as in a conducting target. This barrier can be overcome by

Appendix B (continued)

applying an ac signal at high frequencies. In this range, the electrons oscillating back and forth by the electric field gain sufficient energy to ionize argon atoms. This is in addition to the acceleration away from the target. Since these field-driven electrons generate ions directly, sustaining the plasma does not rely on the secondary electrons emitted from the target. Even though the process seems symmetric considering the cycles, it is asymmetric due to the system geometry.

The Sputtering Guidelines are given as below

1. Check whether the temperature of the cryo pump is below 25 K.
2. Check whether the 4 LED's corresponding to the water supply are 'ON'.
3. Check whether there is enough Argon and Oxygen for the deposition.
4. Check whether the throttle is open and the other valves are closed.
5. Open the "VENT" valve until the PG1 (Pressure Gauge 1) attains atmospheric pressure (Look at the PG1 value in the display)

Note: Due to a minor measurement error, the display would not show 760. The PG1 value stops going up in a predictable way after it reaches a value of around 720-750. Just wait for around 2-3 minutes after a value of around 700-750 is reached before attempting to open the chamber.

Appendix B (continued)

6. Use the controller to open the lid of the sputter chamber to place (or) remove the wafer.
7. Screw down the wafer holder to a comfortable position so that you can keep/remove the wafer.
8. Place/remove the wafer in the holder and screw the holder to its initial position.
9. Clean the chamber and the rim of the chamber with methanol. Lower the lid down to its place and align the lid perfectly to the chamber. Check if the roughing pump is ON otherwise turn ON the pump. Open the "ROUGH" valve. The value of PG1 and PG2 will start going down after the ROUGH valve is opened. PG1 is the chamber pressure. PG2 is the FORLINE pressure. After the value of PG1 comes to around 5×10^{-2} Torr close the ROUGH valve.
10. BURPING PROCESS: If the pressure reduces very slowly (2 points or less), close the Rough valve. Then, open and close the VENT valve (instantaneous open-close). Then open the ROUGH valve again. During this process the PG1 value will go up, to around 3 mTorr and start reducing as soon as the ROUGH valve is opened. Generally the burping process needs to be done twice to get to the desired pressure (5×10^{-2} Torr) range.

Appendix B (continued)

11. Once the PG1 goes down to around 5×10^{-2} Torr, open the "CAPMAN" (Capacitance Manometer) valve and then open the "HIVAC" valve (Disregard the PG1 value after opening the HIVAC valve. PG1 can measure pressure values only up to the range of 10^{-3} Torr).

HI-Vacuum Stage

12. Wait for 30 minutes and check the pressure by pressing IG1 (Ion Gauge 1). IG1 can measure pressures up to 10^{-10} Torr.
13. If the pressure is in the desired range (usually around 2×10^{-6} Torr) press DEGAS. DEGAS is used for getting accurate chamber pressure values.
14. Turn DEGAS off in 1 min and check the pressure.
15. If the pressure is in the desired range, turn OFF the ion gauge and close the throttle valve. Wait till the Throttle valve closes before doing anything else.

Deposition Stage

16. Open the appropriate knobs in the Argon and Oxygen gas bottles to let the gases in the system.
17. Open GAS RING (for oxygen) and appropriate gas (GAS1, GAS 2 or GAS 3 depending upon the target holder used) for passing Argon.

Appendix B (continued)

18. Turn ON MKS 247(4- channel gas controller) and open the appropriate gas channels.
19. Turn on the MKS 250 (pressure read out unit) for maintaining the gas ratio and gas pressure.
20. Adjust the respective flow meters for the correct flow of the gases (standard values- 18.5 sccm Argon and 1.5 sccm oxygen [90/10 ratio]). The MKS 250 values will hover around 1.000 (corresponding to around 20 mTorr pressure). Check PG1 also for chamber pressure values.
21. Check whether the RF power cable is connected to the appropriate gun.
22. Switch on the RF switch on the back of the console. Turn ON the "Tuner module" and then turn on the RF power display unit.
23. Slowly ramp up the RF power (one watt every 3 seconds) to around 15 W and usually plasma will be generated in the chamber accompanied by an increase in the DC bias values. If the reflected power value is high (>5 W) ramp up till the output power is 30 watts and then open the shutter 1,2 or 3 (depending upon where your target is) the reflected power value should come down to zero. Now close the shutter. Continue ramping up the RF power until you reach the desired

Appendix B (continued)

value (standard value – 200 W). If necessary “pre-sputter” for a desired amount of time (usually 30 min).

24. Set the heater temperature by pressing “up” and “down” arrows until you get to the desired temperature (Standard Value - 600°C).

25. Then hit “START” to ramp up the temperature and wait till the desired temperature value is reached.

26. Open the appropriate shutter by turning Shutter1, 2 or 3 Knobs.

27. Turn on the substrate rotator switch (DART switch) to expose the plasma to the wafer.

28. This starts the deposition. Note the deposition time. Keep monitoring the RF reflected power every 10-15 minutes to see if the reflected power is going up or fluctuating too much.

After the deposition is done

29. Close the appropriate target shutter first.

30. Turn OFF the substrate rotor (DART Switch).

31. Hit STOP button to reduce the heater temperature.

32. Slowly ramp down the RF power (one watt for every 3 seconds) to 0 W and then turn off RF switch. Turn off the tuner module and the RF supply switch in the back of the console.

33. Turn OFF the MKS 250 unit

Appendix B (continued)

34. Turn OFF the appropriate channel for the gas and the MKS 247 flow controller and turn off the flow controller.
35. Close the appropriate GAS valves on the front console.
36. Open Throttle and wait till it opens and then close HIVAC valve.
37. Close "CAP MAN".
38. Check whether temperature is below 30°C and then open the VENT valve (very important). It usually takes around one hour for the temperature to go down to 30°C.
39. Open chamber and take your sample out.
40. Repeat steps 6- 13 to make sure the chamber is not exposed to atmosphere. It is not necessary to reduce the chamber pressure to 5×10^{-2} Torr unless you are immediately doing another deposition. So close the ROUGH valve after PG1 values are around 300 Torr.

Appendix C Sol-gel Preparation of Barium Strontium Titanate

Sol-gel preparation: initially 7.67 gm barium acetate was added to 40ml Acetic acid and mixed till it was dissolved in it. Then 4.3 gm strontium acetate was added to 40ml of Acetic acid separately and mixed till it was dissolved. Then the two solutions were mixed together for sometime to ensure an equilibrium room temperature was achieved. This solution was then refluxed at 100°C for 5hrs. After 5hrs of continuous mixing, the solution was let to cool down to room temperature. Failure to bring the solution to room temperature and adding TiNOP to it can cause early precipitation of the sol-gel.

In another beaker 12.66ml Titanium isopropoxide was added to 10ml of 2-propanol solvent. Care was taken to ensure that absolutely no water was present on any of the measuring cylinders or beakers while mixing since TiNOP tends to precipitate if it comes in contact with water. The TiNOP+propanol solution was added to the Ba+Sr+acetic acid solution at room temperature. This solution was left for mixing at room temperature for about 10hrs. The solution was stored in conical flasks after thoroughly cleaning and drying them with Nitrogen to ensure no water molecules are present inside the container. The conical storage flask with BST sol-gel was refrigerated for around 12hrs before it could be used.

Spin-coating recipe: The samples to be coated with BST sol-gel were cleaned using standard RCA cleaning procedure. They were also cleaned

Appendix C (continued)

using DI water, acetone, methanol and IPA solutions just prior to BST deposition followed by N₂ drying. The cleaned samples were put on a hot plate for thorough drying at a temperature of 100°C for 10mins. The sample was then placed on the spin coater and a few drops of refrigerated BST sol-gel were drop cast on the sample to ensure full area coverage. The spinning speed was set at 2400rpm and time to 40sec. The spinning speed and time were selected for optimum thickness requirements. After the spinning, samples were again placed on the hot plate at 150°C for 10mins as soft bake to get rid of organics in the solution. The samples were annealed at different temperatures, durations and ambients as described in chapter 3.

Appendix D Microfabrication of Interdigitated Devices for RF Measurements

Sample preparation (experimental matrix) for the samples is given below. A total of 16 substrates were deposited with BST (60/40) with the following conditions. Substrate specifications are given as below:

- Number of Silicon samples - 2
 - B1: no anneal (center) – thickness - ~330nm
 - B2: no anneal (right side bottom corner) – thickness - ~280nm
- Number of Alumina samples - 6
 - B3: anneal in Air (right side)
 - B4: anneal in Air (left side top corner)
 - B5: anneal in O₂ (left side corner)
 - B6: anneal in O₂ (Bottom row center)
 - B7: anneal in O₂ (left side bottom corner)
 - B8: no anneal (for XRD)
- Number of sapphire samples - 4
 - B9: anneal in Air (center)
 - B10: anneal in O₂ (right side top corner)
 - B11: anneal in O₂ (right side row center)
 - B12: no anneal (for XRD)

Appendix D (continued)

- Number of MgO samples - 4
 - B13: anneal in Air (top row center)
 - B14: anneal in O₂ (center)
 - B15: anneal in O₂ (left row center)
 - B16: no anneal (bottom row center)

The patterning procedure for the above samples is as follows (adapted from Tony Price's previous trials [35]):

1. Cleaning Samples

- a. Clean with acetone and methanol, then N₂ dry
- b. Dehydration bake on hotplate at 115 C for 5 minutes. Let it cool for a couple of minutes before spin-coating with resist.

2. Patterning 1827 Positive Resist

- a. Be sure to put down black colored dicing saw tape on Quintel chuck if using transparent substrates.
- b. Spin HMDS at 3000rpm for 30 seconds.
- c. Spin 1827 at 3000rpm for 30 seconds.
- d. Bake on hotplate at 90°C for 90 seconds.

Appendix D (continued)

- e. Expose for 10 seconds on Quintel mask aligner (lamp intensity was at 18.5 mW/cm^2 when recipe was derived).
 - f. Develop for 30 - 40 second (or longer if necessary) in MF319 or AZ-726.
 - g. Descum for 2 minutes in O_2 , using brown box asher at 50-75W (It's difficult to tune right at 50W). Or the plasma therm can be used: O_2 , flow rate of 99 sccm, pressure of 300 mT, power of 75 Watts. I used the plasms therm since the asher was down. No Hardbake, resist should etch at $\sim \text{nm/min}$ in DRIE.
3. Determining BST thickness
- a. Pattern 1827resist on the Si/BST sample (the one that was not annealed).
 - b. Submerge the sample in 10:1 BOE to etch the BST film.
 - c. Observe the sample while it is in the BOE. When it appears that the BST has been etched (you should be able to clearly see the silicon substrate in the areas in which there is no photoresist), take the sample out of the BOE. It took around 11mins to etch through the annealed BST in 10:1 BOE.
 - d. Place it in DI water for 1min and then N_2 dry.

Appendix D (continued)

- e. Observe the sample using a microscope to ensure that the BST film has been removed from the field.
 - f. Rinse the sample with acetone and methanol to remove the 1827 resist. If that doesn't work, then use 1165 resist remover at 80°C for ~20 minutes.
 - g. Determine thickness of the non-annealed BST using a profilometer.
 - h. Measurements for silicon samples – B1 – ~330nm and B2 – ~280nm.
4. Etching BST using DRIE for non-silicon samples using Pyrex recipe
- a. RF 2800W (13.5MHz)
 - b. Bias: 550W
 - c. C4F8: 17sccm
 - d. CH4: 13 sccm
 - e. Argon: 100sccm
 - f. Temp: -20C
 - g. Substrate distance from source: 140mm

Appendix D (continued)

Once the samples have patterned 1827 on them, measure the thickness of the patterned resist using a profilometer.

- a. Run the pyrex DRIE recipe for 1-2 min and then take more profilometer measurements. The step that is being measured in this case consists of resist and patterned BST.
- b. Strip the resist from the sample by putting it in the brown box asher (up to 30 min) or by using the plasma therm.
- c. Take more profilometer measurements. This time, only the step height of the BST is being measured since the resist has been removed.
- d. Use $\text{etch rate} = \text{Measurement D} / \text{experimental etch time}$ to calculate the etch rate of the BST film.

The etch rates for BST thin film samples on different substrates is given in table 10.

Table A. Etch rates for BST thin film samples on different substrates

Type of Substrate	Air anneal	Oxygen anneal
Alumina	56nm/min	50nm/min
Sapphire	60nm/min	55nm/min

Appendix D (continued)

Calculate the time required to etch through the total film by using, total etch time = Measurement A/etch rate. (Based on film thickness determined from silicon sample)

1. Once the total etch time required is known, use this time to etch the BST films on the remainder of the samples.
2. Strip the remaining resist by putting samples in the brown box asher at 150 Watts for up to 30 minutes. Since the asher was not working I used the DRIE O₂ clean recipe for 5mins (not recommended by Rich).

Side notes to consider while following the said recipe:

- Films grown on different substrate materials will have different characteristics and will etch at different rates. Also, if the annealing conditions are different, the etch rates will vary. Therefore, the above procedure needs to be carried out for each substrate material used along with each annealing condition used.
- Since the resist has been exposed to plasma during the DRIE process, it will be very difficult to remove with acetone and methanol. This is why it is best to put it in the asher or plasma therm or use DRIE O₂ clean recipe to get rid of any resist residue.

Appendix D (continued)

5. Patterning 3000PY (NR-1) Resist

- a. Spin coat 3000PY at 3krpm for 30 seconds (resist thickness: ~2.5um)
- b. Pre-exposure bake at 155C for 90 seconds
- c. Expose for 11 seconds (lamp intensity on Quintel was down to 18.8 mW/cm² at the time)
- d. Bake at 110C for 60 seconds
- e. Develop in RD6 for 7seconds
- f. Descum for 2 minutes in O₂, flow rate of 99 sccm, pressure of 300 mT in plasma therm or 60W in brown box asher for 2 min (etch rate: 66nm/min)

6. Lift Off

- a. Lift-off 3000PY and excess metal using RR41 at temperature of 110 C for at least 20 minutes. I needed somewhere around 25mins.
- b. USB clean as needed (up to 10 – 15 minutes) while samples are submerged in acetone.

Appendix D (continued)

Metal Deposition (using thermal evaporator) 3 or 4 pellets should give at least 1um. Table 11 gives details of thermal metal deposition conditions for chromium and gold electrodes.

Table B. Metal deposition conditions for Cr and Au

Metal	Rate	Current	Displayed Thickness	Actual Thickness
Cr	0.3 – 0.4 A/s	~50Amps	0.15kA or 15nm	--
Au	0.4 – 0.5 A/s (0-100A)	190 Amps	5.3kA or 530nm	4.7kA or 400nm
	3 A/s (100 – 1000A)	210 Amps	10.06 kA or 1um	7.8kA or 780nm
	6.5 A/s (1000 – max)	220 Amps	12kA or 1.2um	9.1 kA or 912nm

About the Author

The author, Ms. Supriya Ashok Ketkar, joined the University of South Florida in year 2006 for the Doctorate program in the Electrical Engineering department. She received her Master's degree from University of Pune, India. Her work as a Research Assistant at The Center for Materials for Electronic Technology (C-MET, Pune; India) led to a very thorough understanding of photoimageable thick film pastes and their electrical properties. She has several peer-reviewed journal publications in the field encompassing electronic packaging and material science. She is a winner of several presentation awards at international conferences. Supriya is a recipient of the MEMS fellowship from USF and has been an NSF funded Graduate Research Assistant for the past 4 years. Her current research work involves the efficient use of BST thin films in frequency tunable and electrochemical supercapacitor applications.